FIG. 1

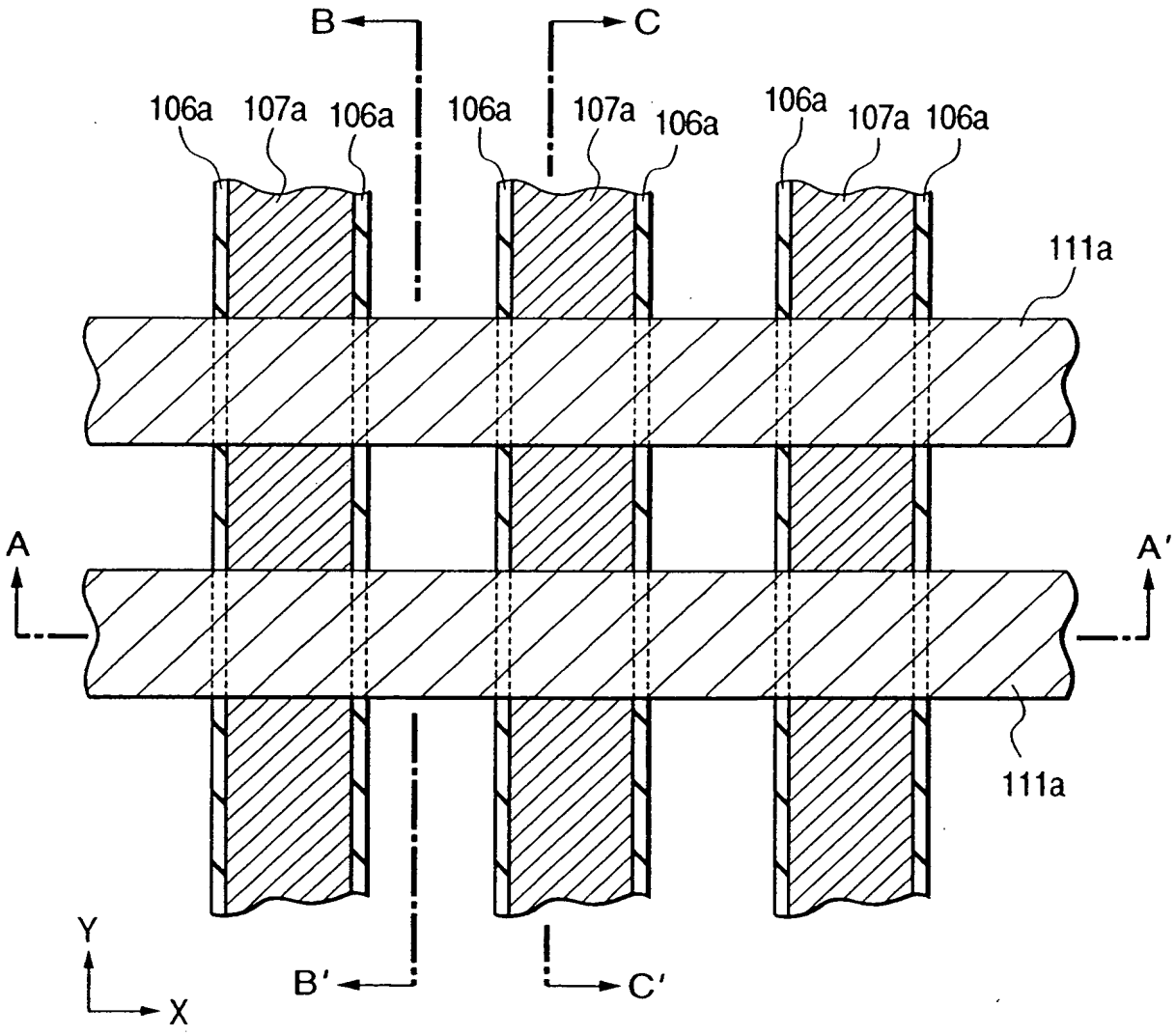

B
C
106a
107a
106a
106a
107a
106a
106a
107a
106a
111a
A
A'
111a
Y
X
B'
C'

FIG. 2A

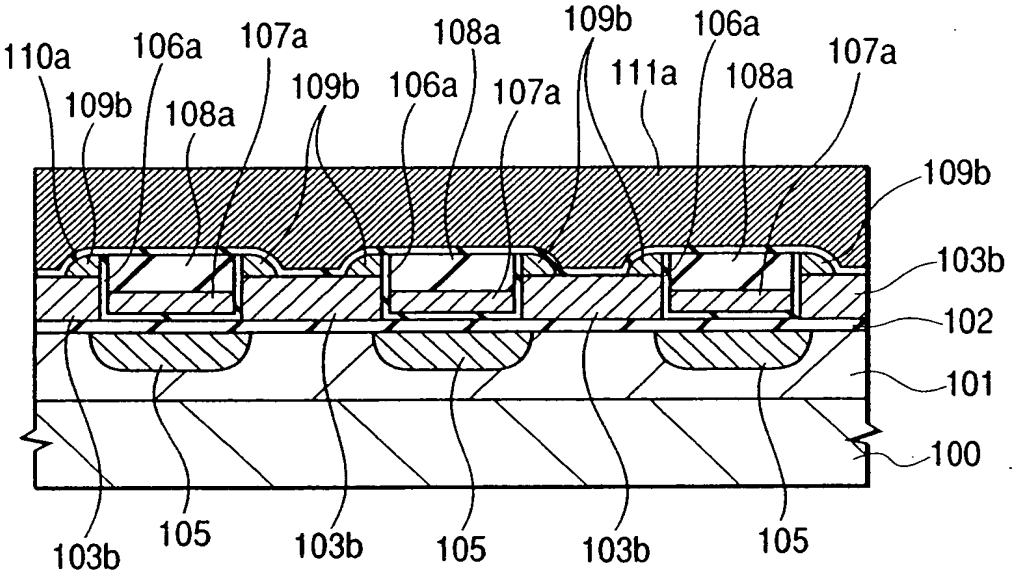


FIG. 2B

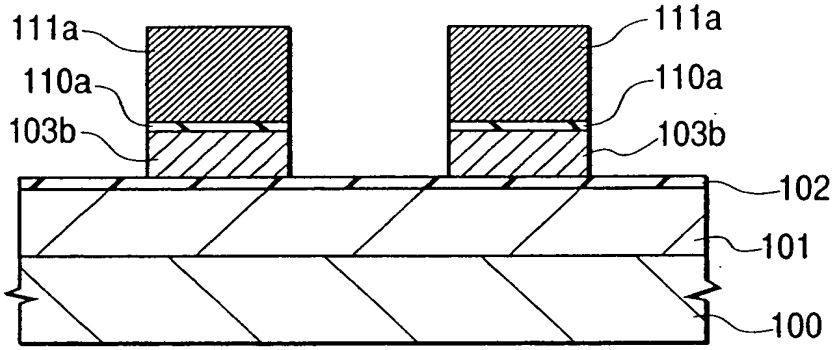


FIG. 2C

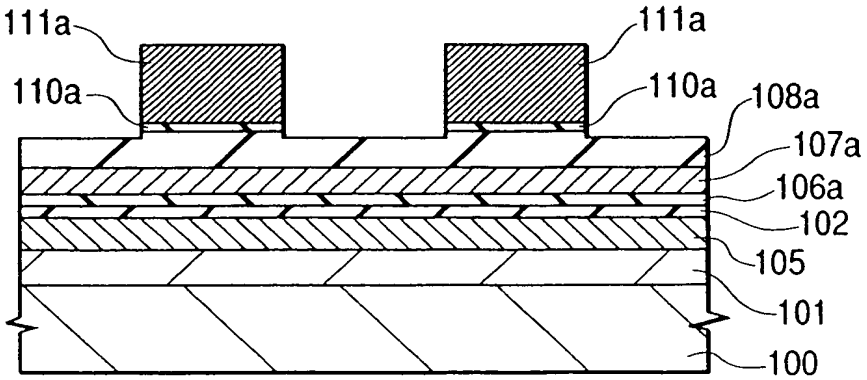


FIG. 3A

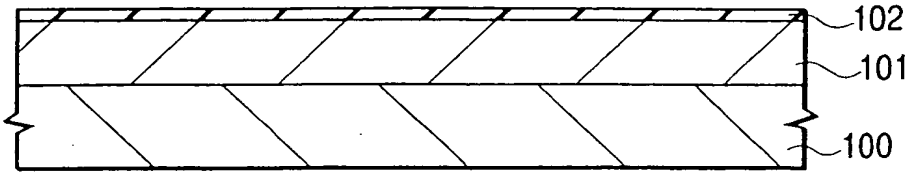


FIG. 3B

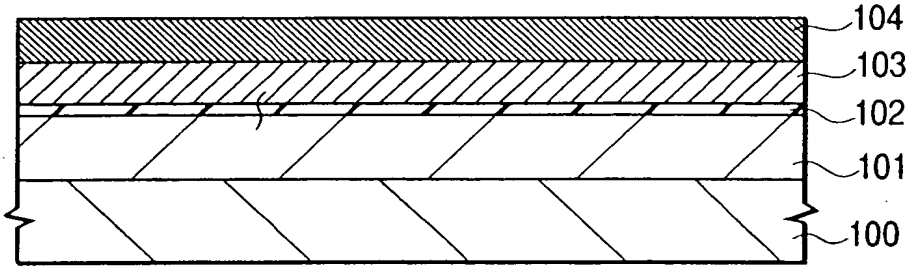


FIG. 3C

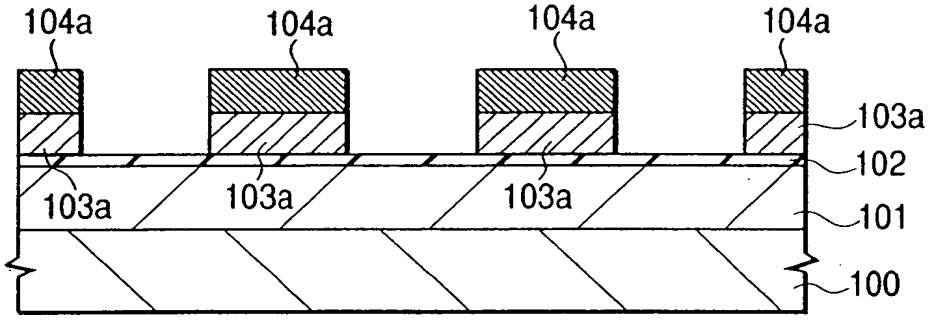


FIG. 3D

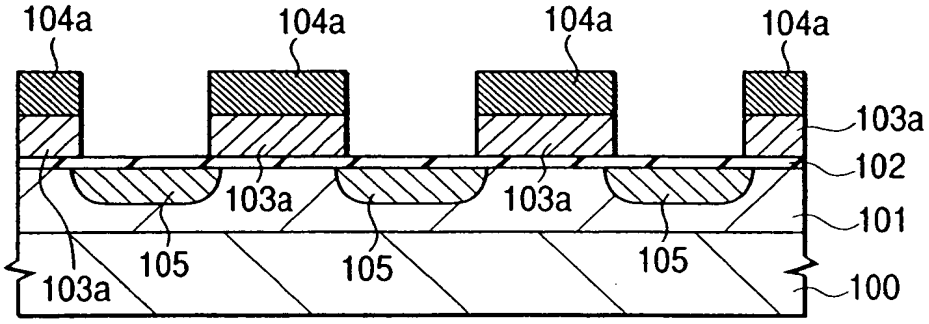


FIG. 3E

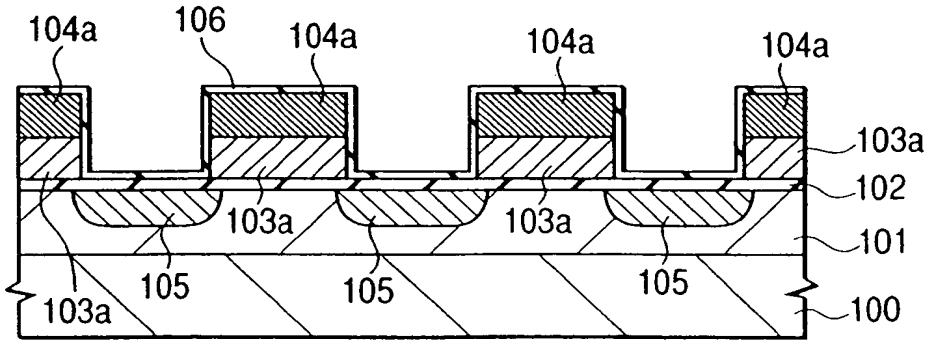


FIG. 4A

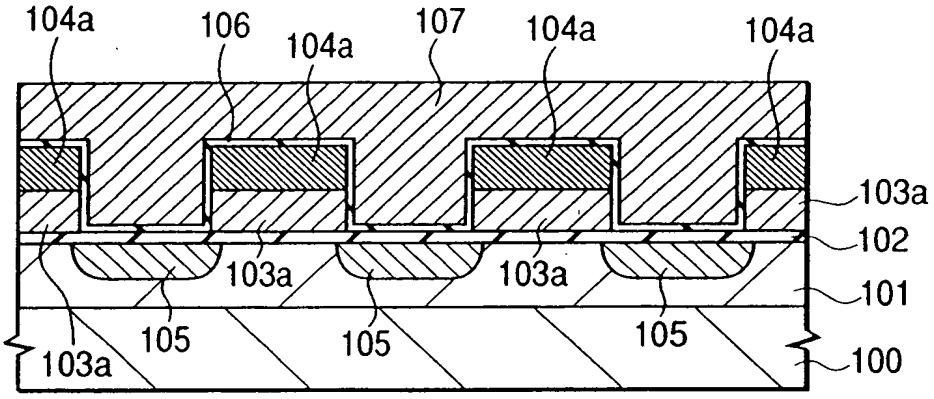


FIG. 4B

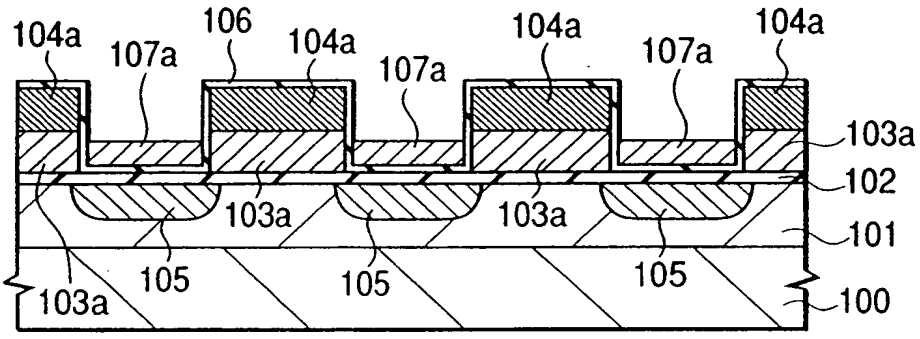


FIG. 4C

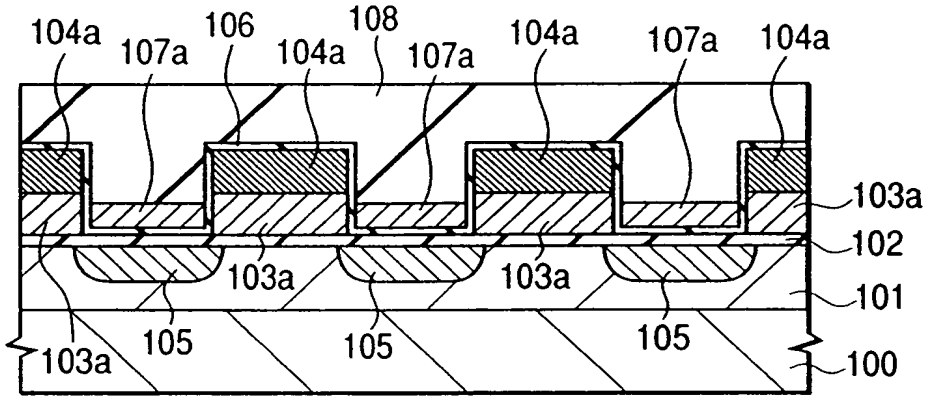


FIG. 4D

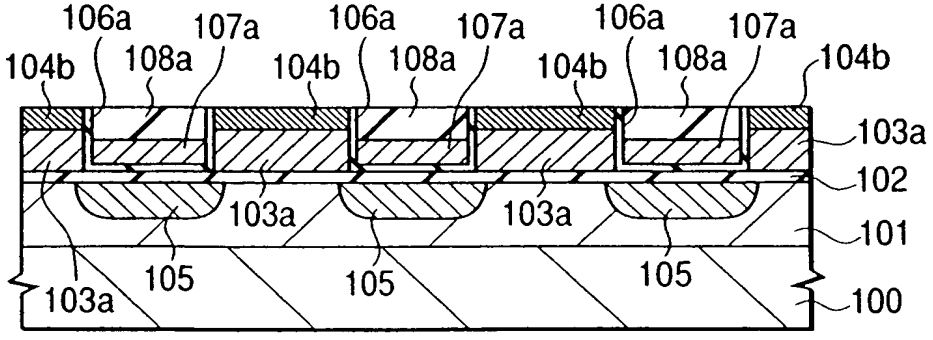


FIG. 5A

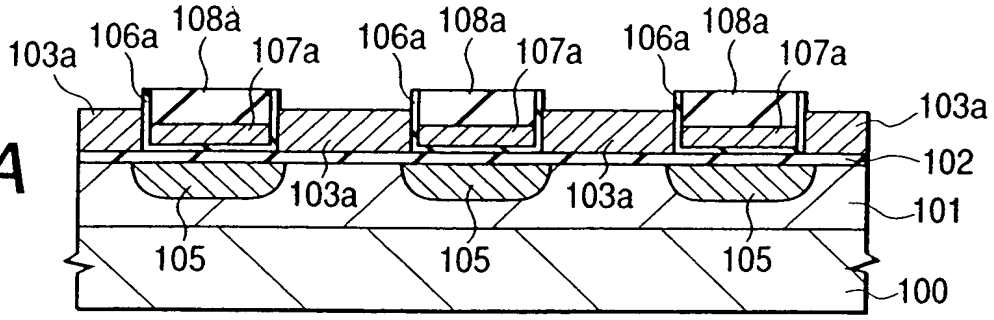


FIG. 5B

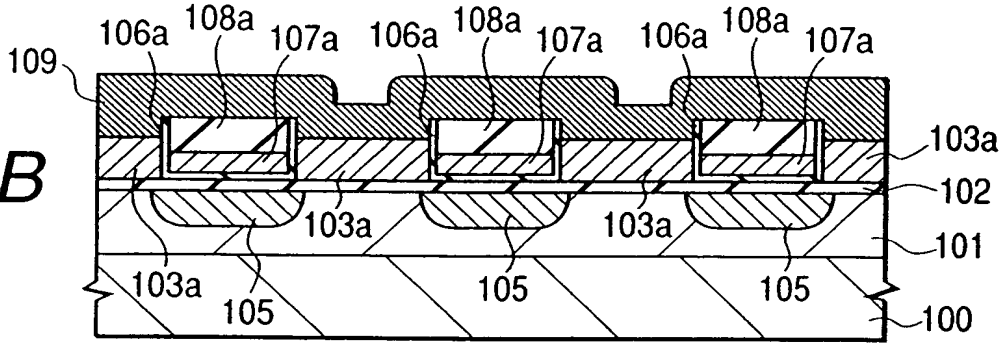


FIG. 5C

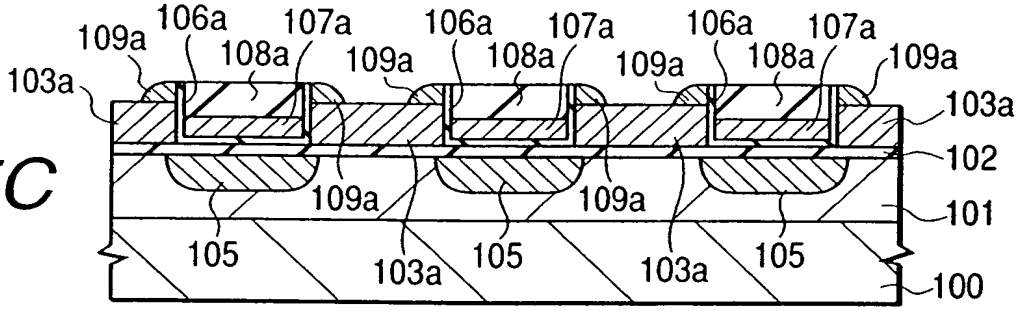


FIG. 5D

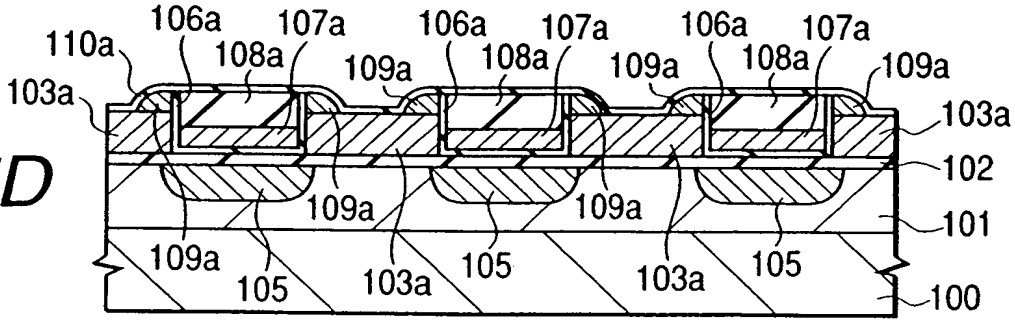


FIG. 5E

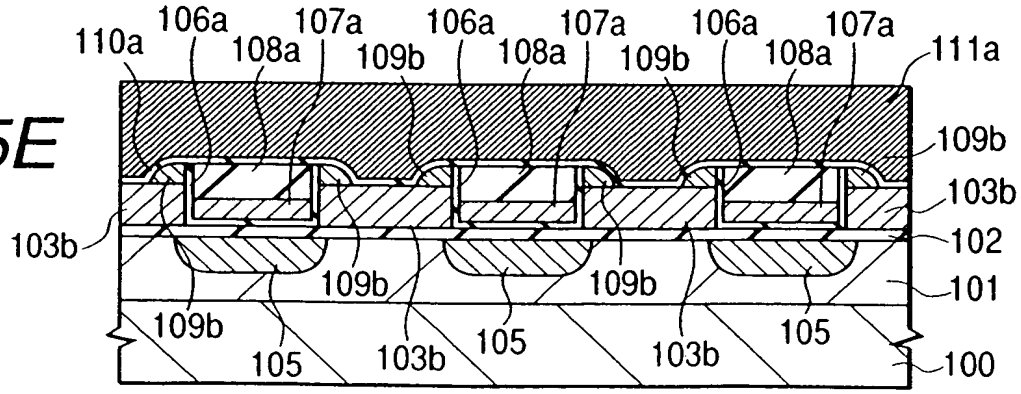


FIG. 6

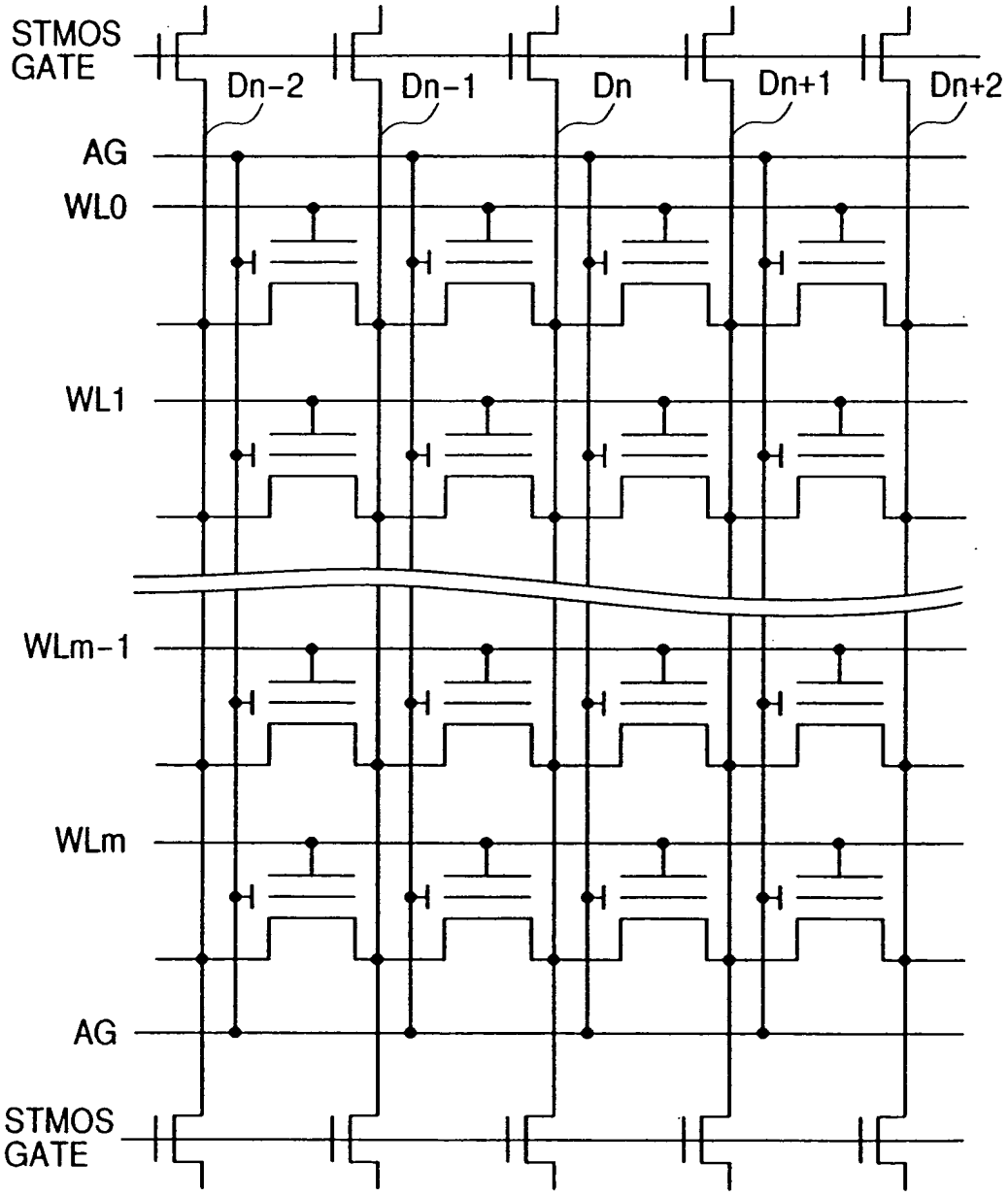


FIG. 7

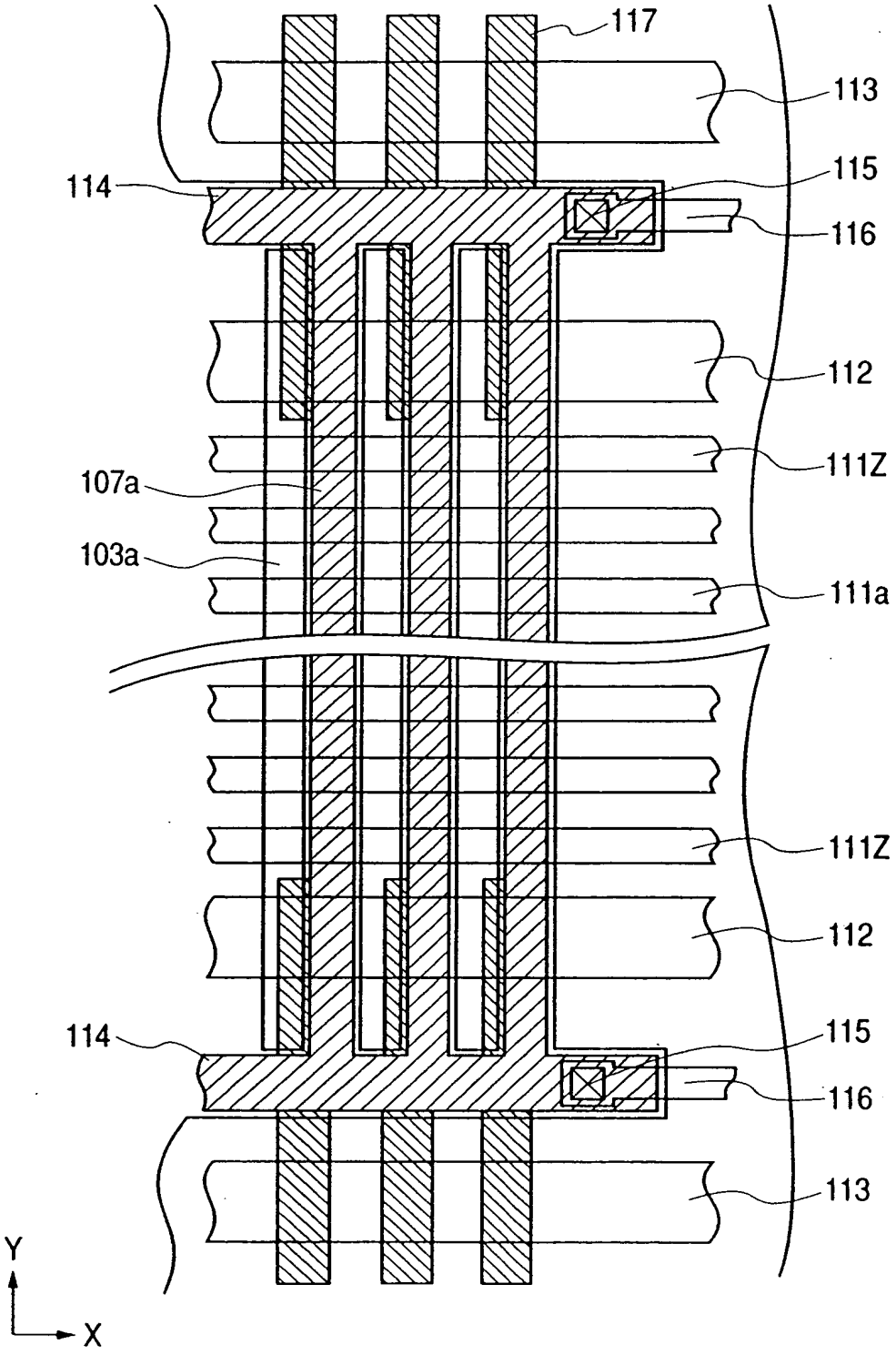

117
113
114
115
116
112
111Z
107a
103a
111a
111Z
112
114
115
116
113
Y
X

FIG. 8

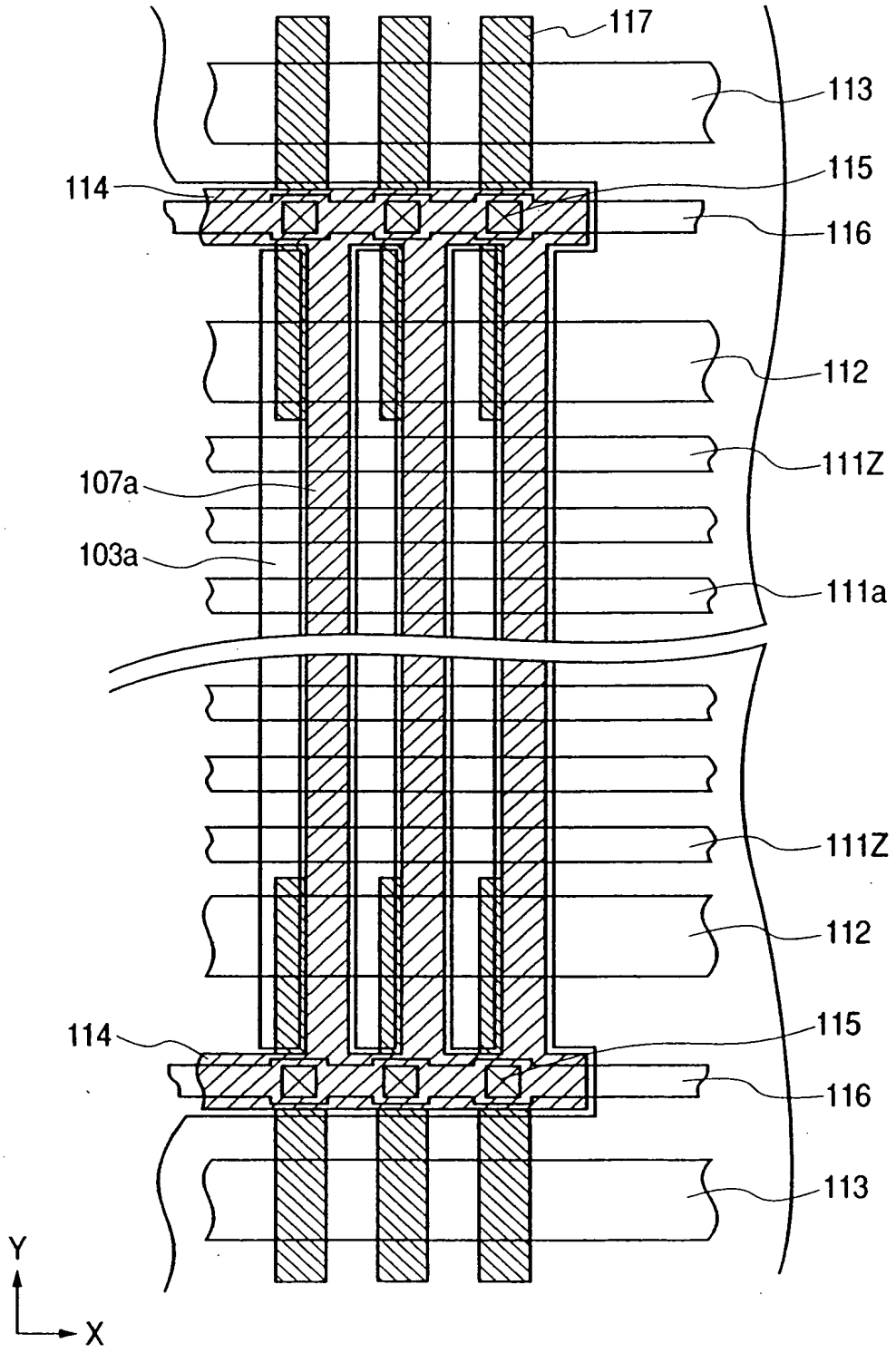

117
113
114
115
116
112
111Z
107a
103a
111a
111Z
112
114
115
116
113
Y
X

FIG. 9

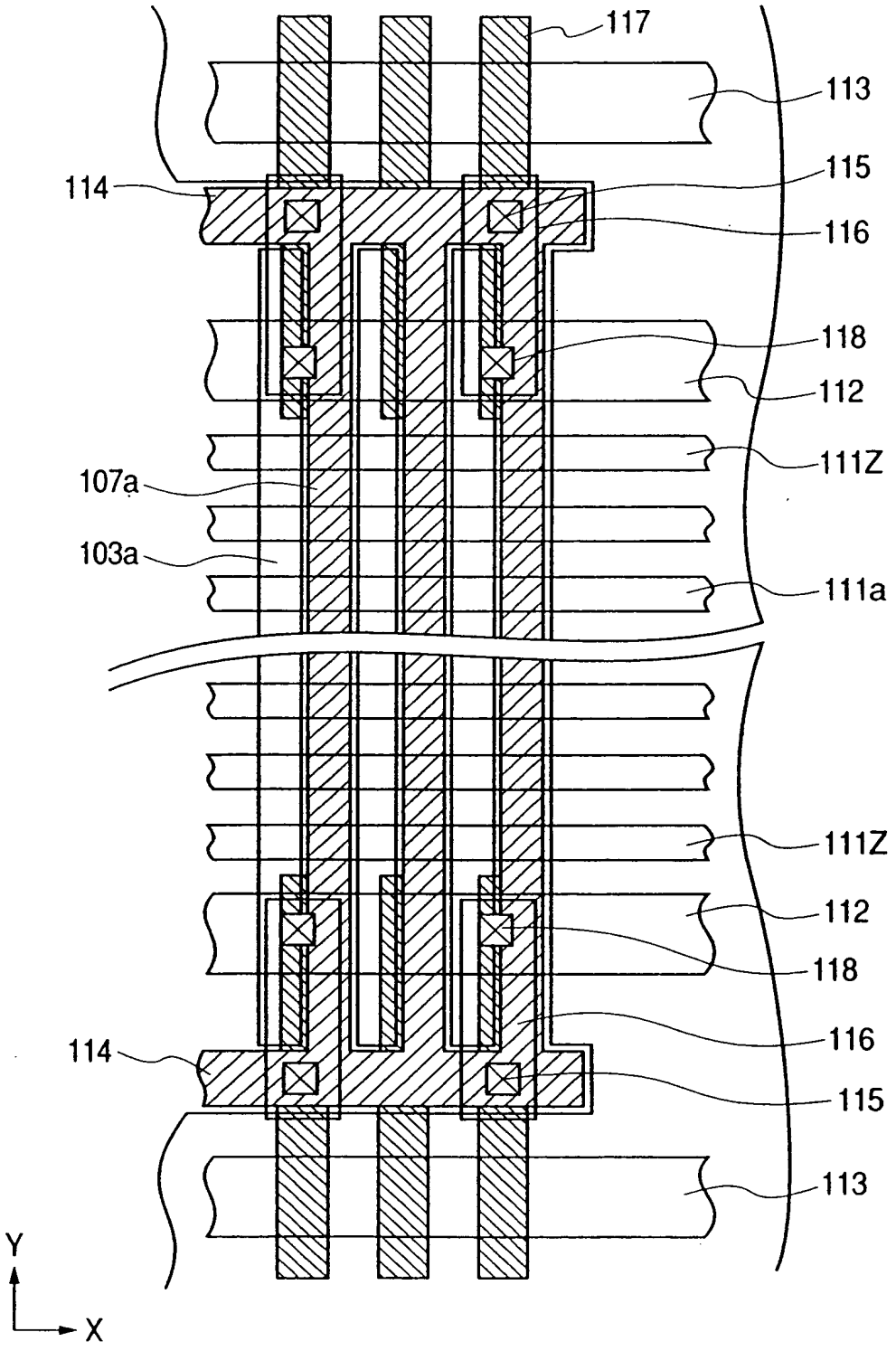

117
113
115
114
116
118
112
111Z
107a
103a
111a
111Z
112
118
116
114
115
113
Y
X

FIG. 10

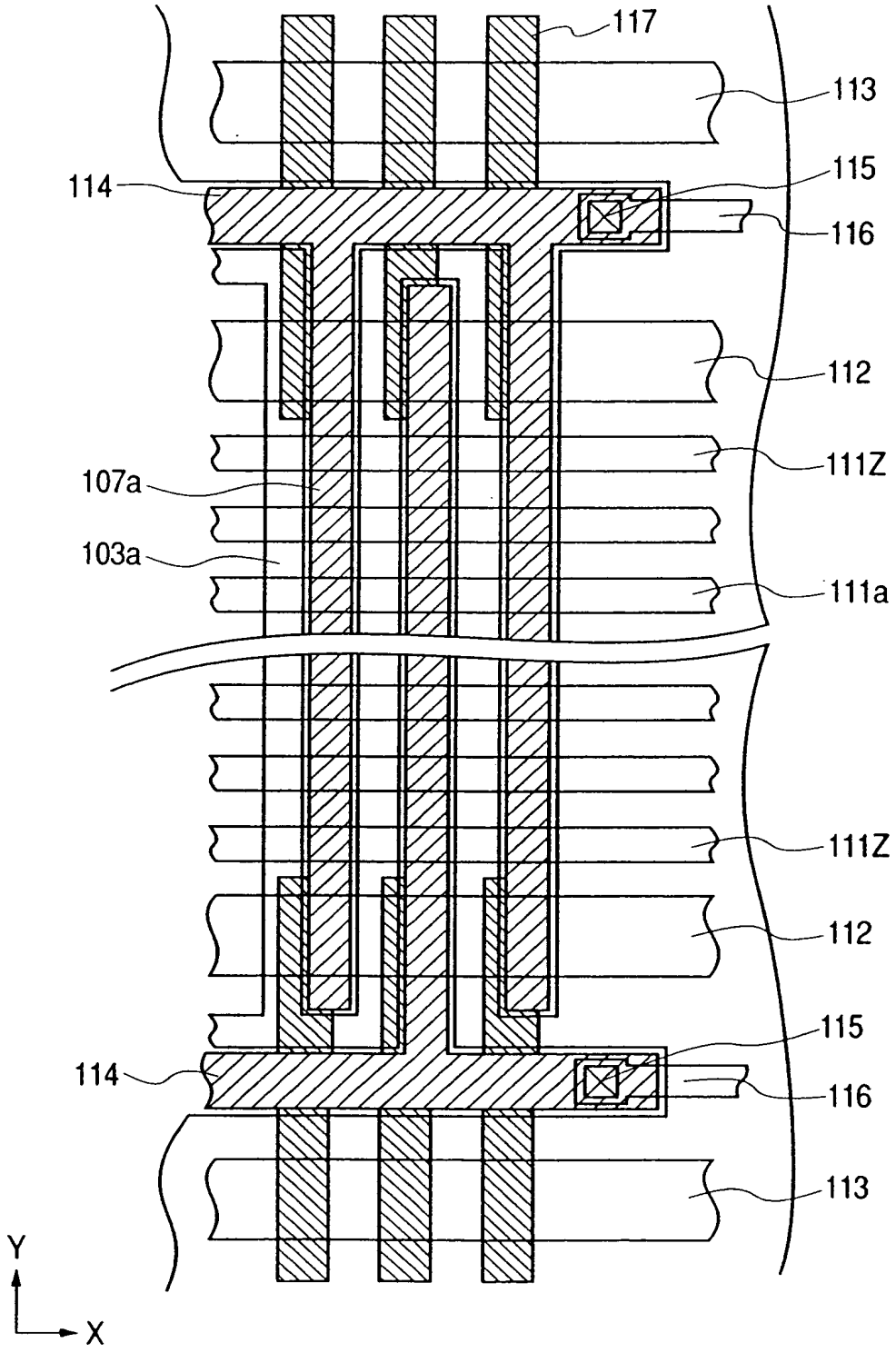

117
113
115
114
116
112
111Z
107a
103a
111a
111Z
112
115
114
116
113
Y
X

FIG. 11

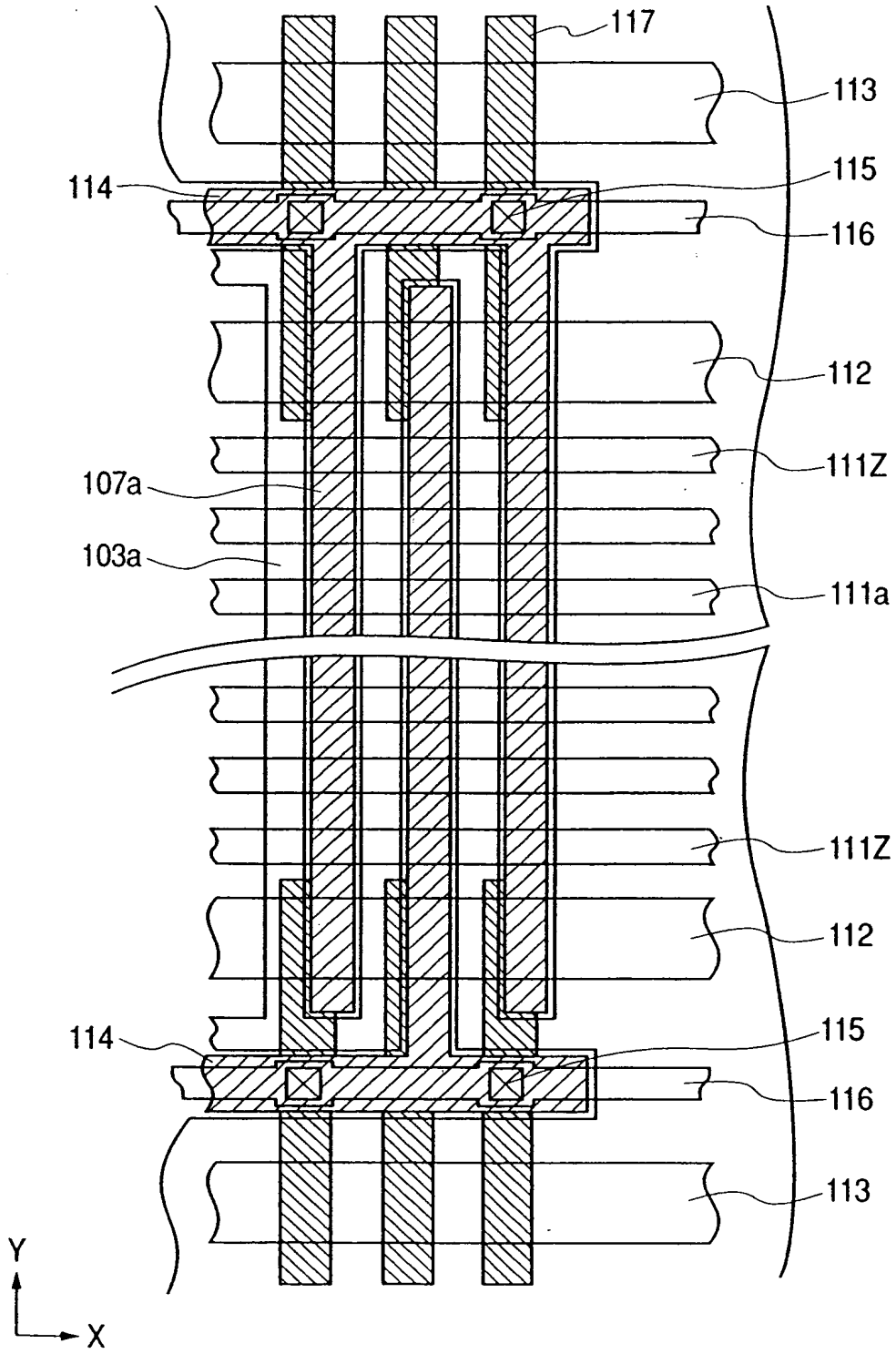

117
113
114
115
116
112
111Z
107a
103a
111a
111Z
112
114
115
116
113
Y
X

FIG. 12

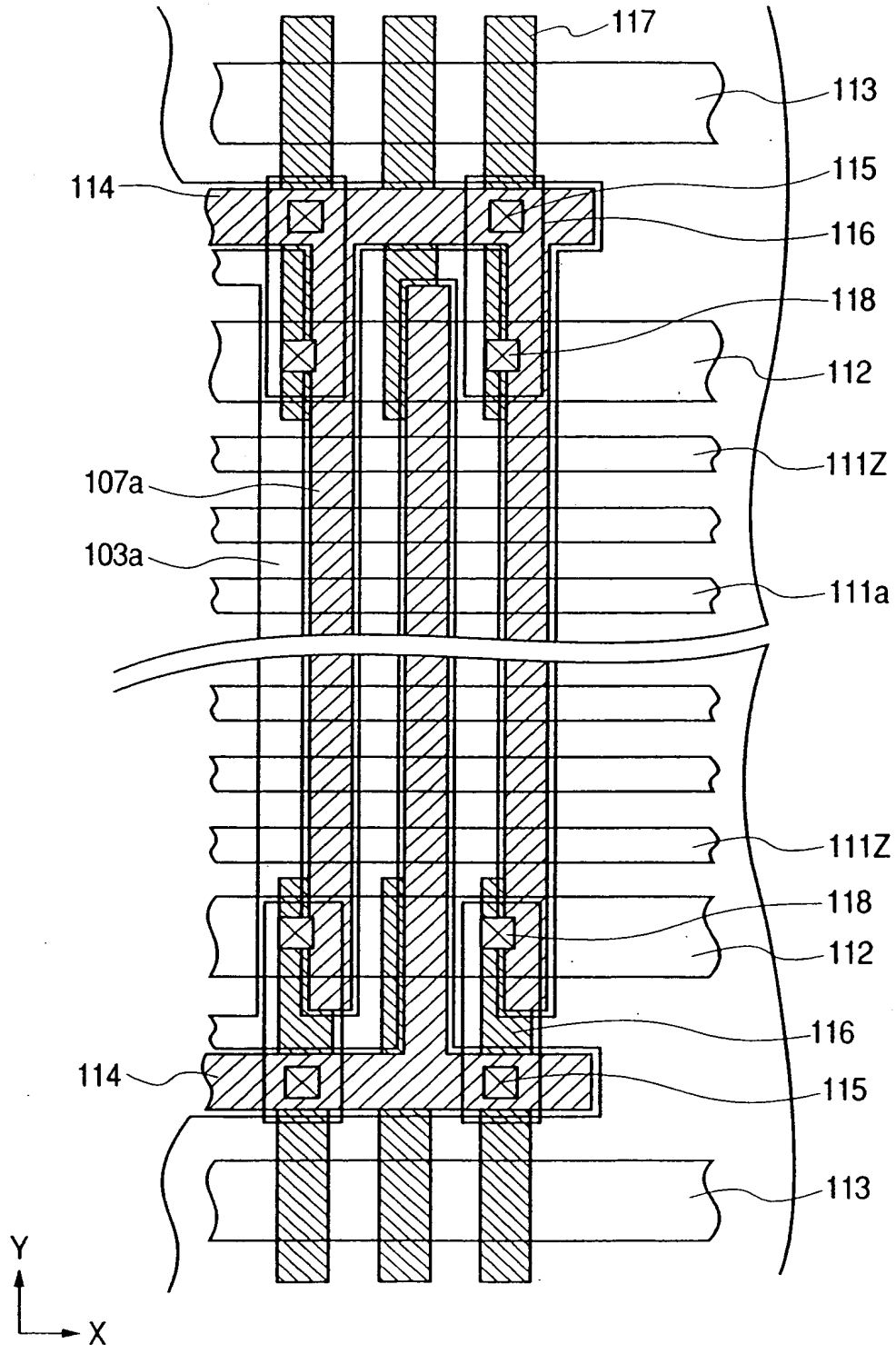

117
113
114
115
116
118
112
111Z
107a
103a
111a
111Z
118
112
116
114
115
113
Y
X

FIG. 13A

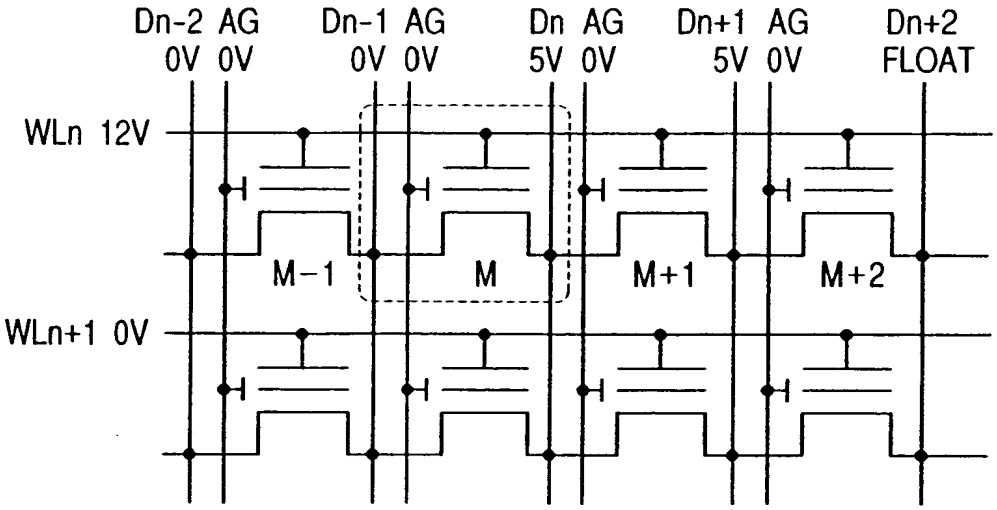


FIG. 13B

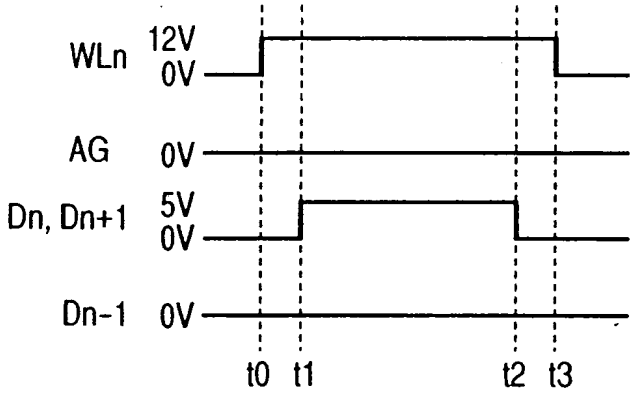


FIG. 13C

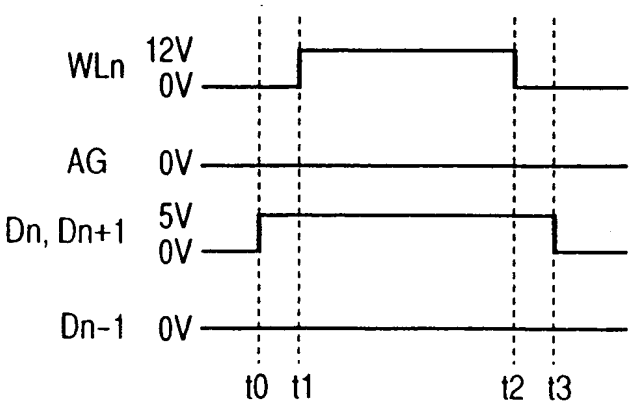


FIG. 14A

ERASE OPERATION VOLTAGE

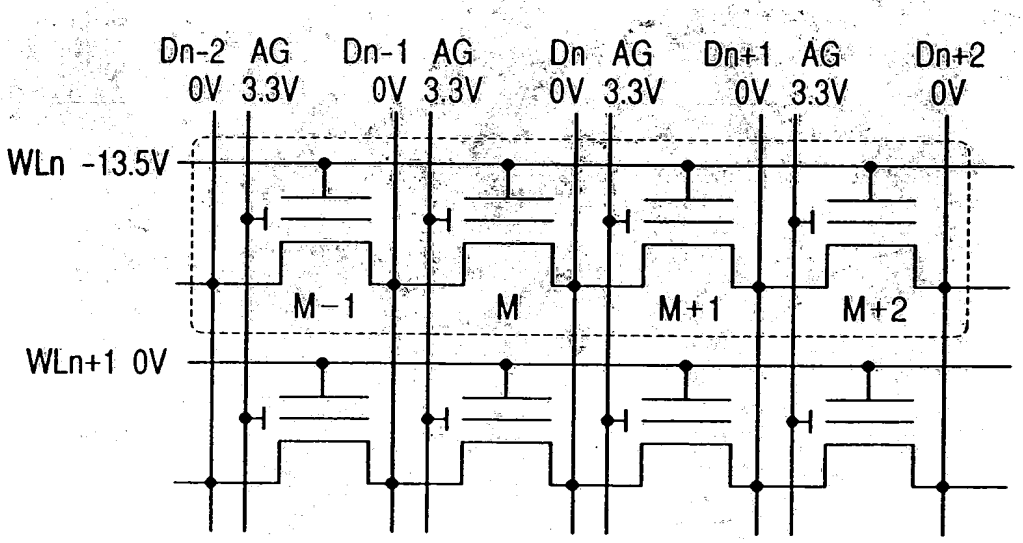


FIG. 14B

TIMING 1

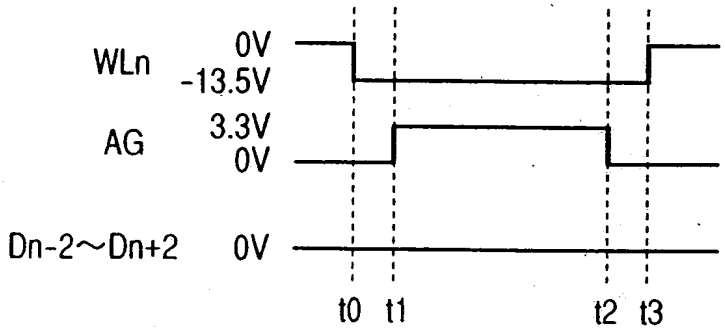


FIG. 15A

READ OPERATION VOLTAGE

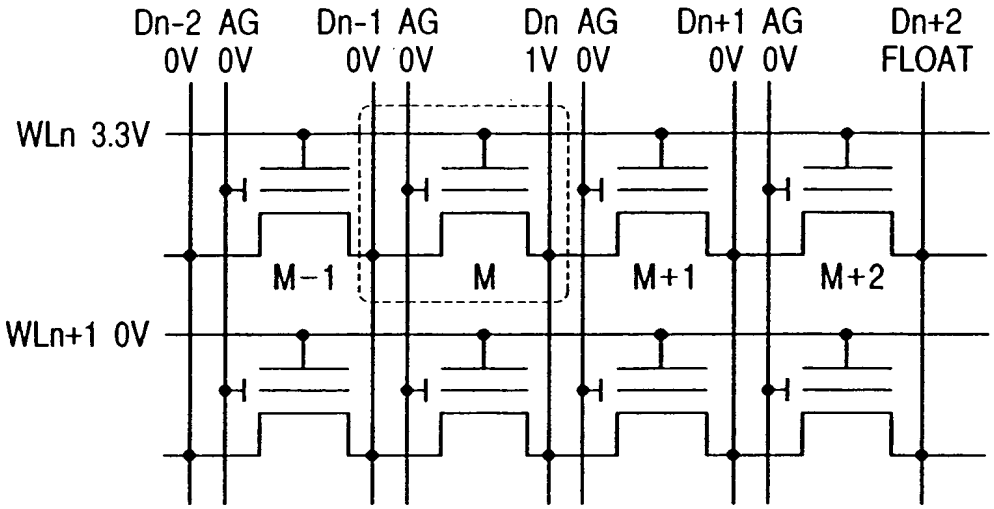


FIG. 15B

TIMING 1

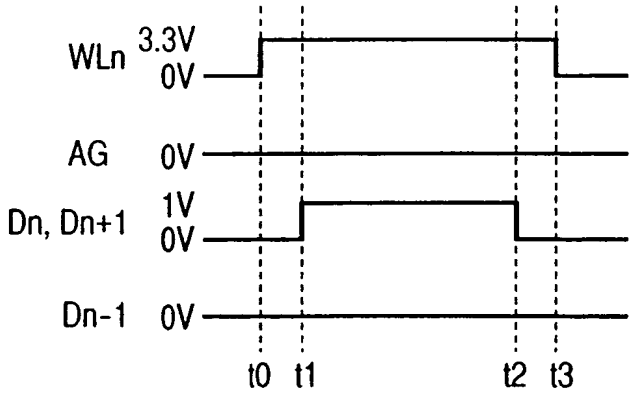


FIG. 15C

TIMING 2

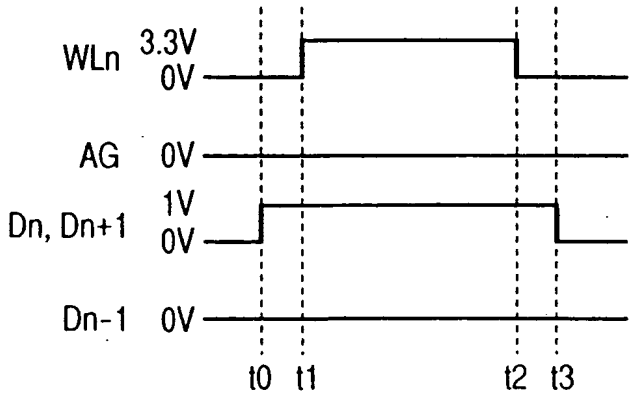


FIG. 16A

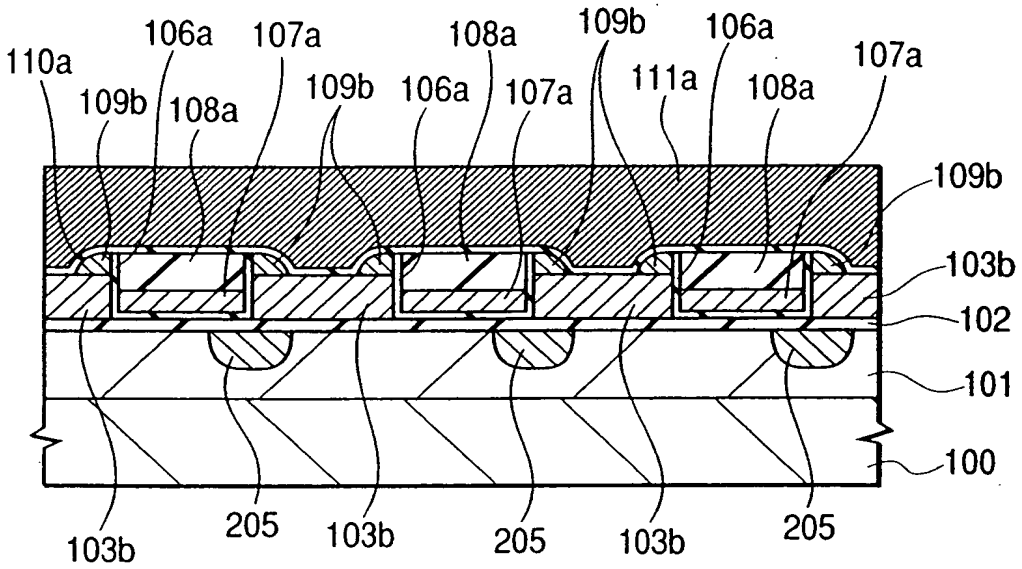


FIG. 16B

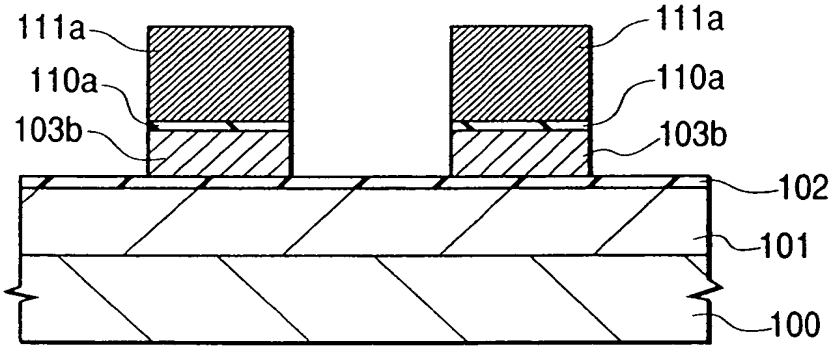


FIG. 16C

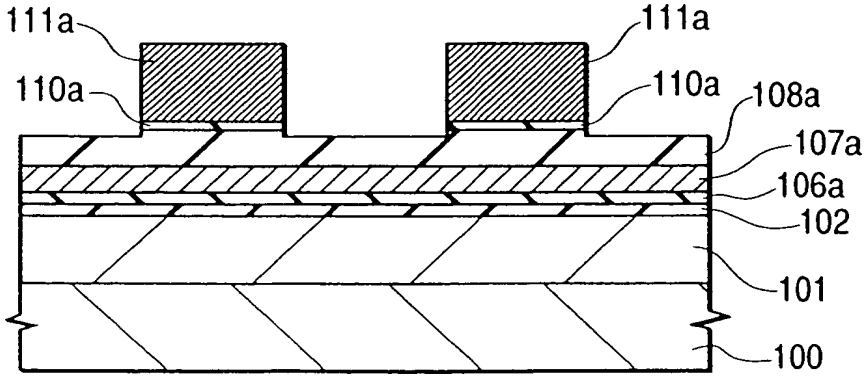


FIG. 17

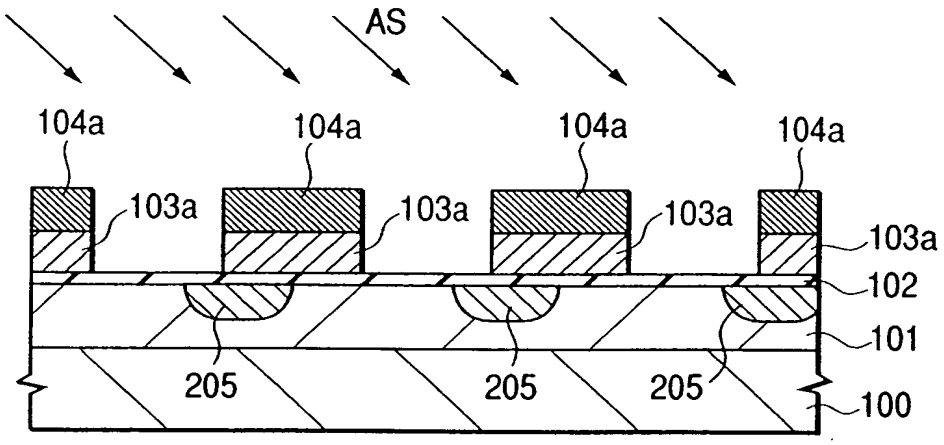

AS
104a
104a
104a
104a
103a
103a
103a
103a
102
101
205
205
205
100

FIG. 18

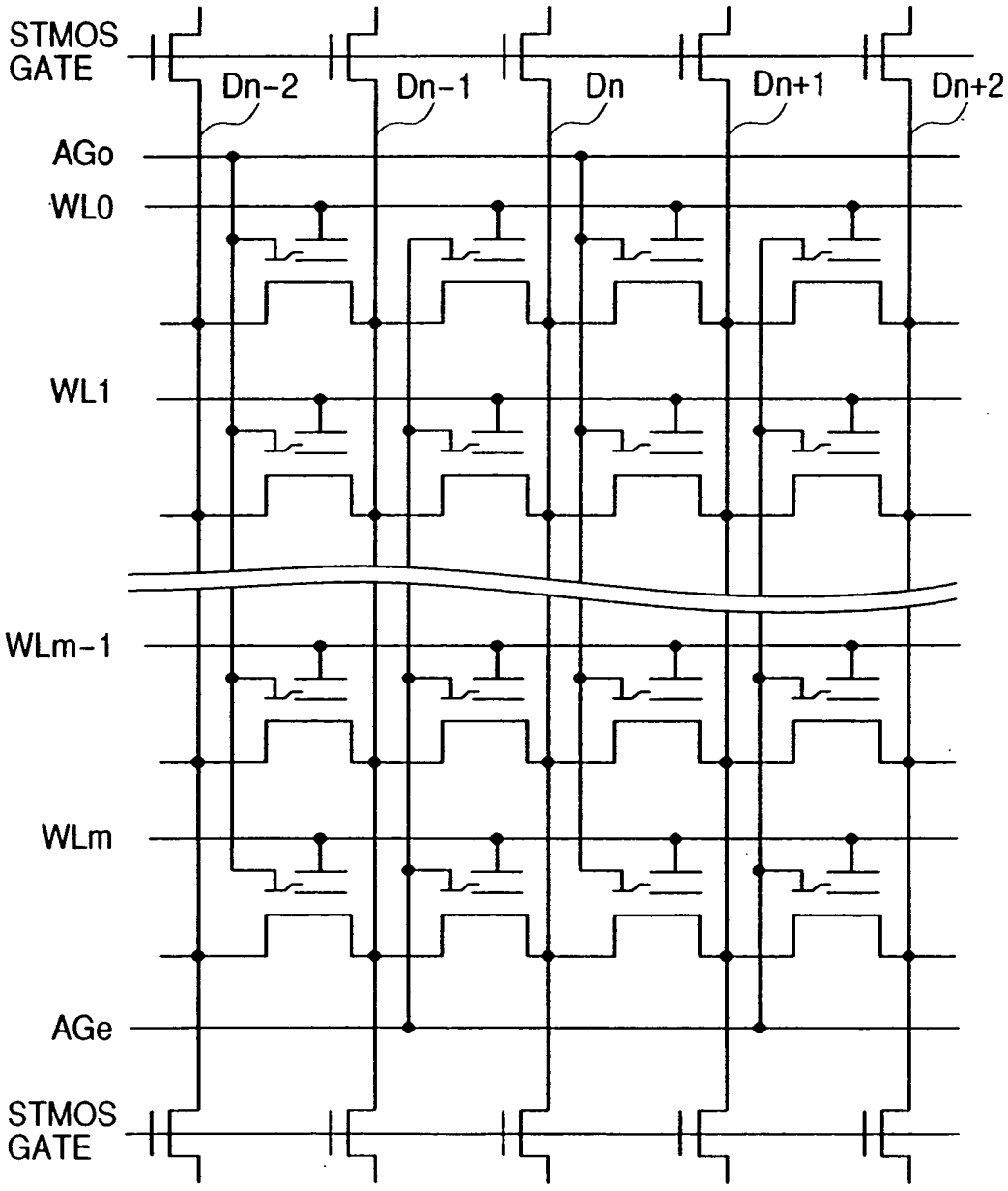

STMOS GATE
Dn-2
Dn-1
Dn
Dn+1
Dn+2
AGo
WL0
WL1
WLm-1
WLm
AGe
STMOS GATE

FIG. 19A

PROGRAM OPERATION VOLTAGE

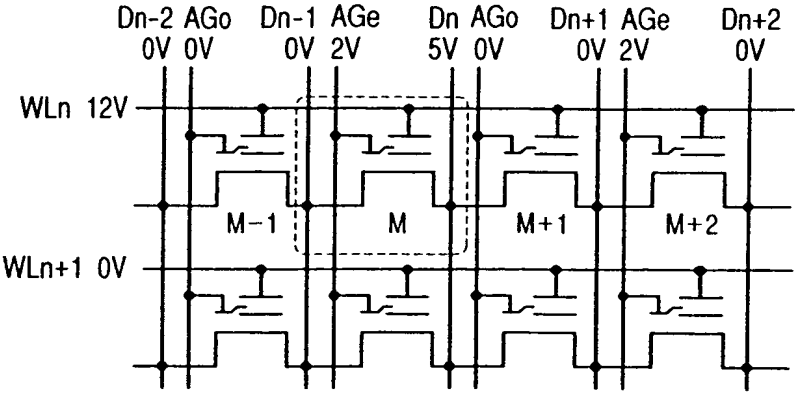


FIG. 19B

TIMING 1

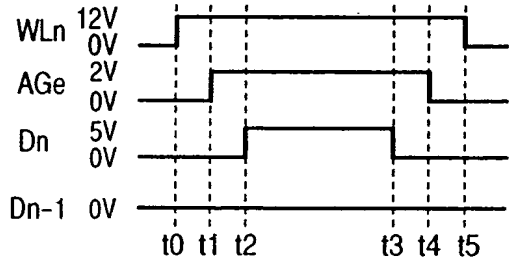


FIG. 19C

TIMING 2

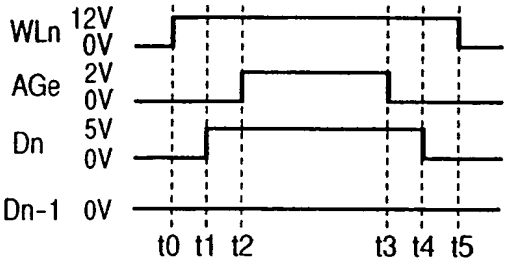


FIG. 19D

TIMING 3

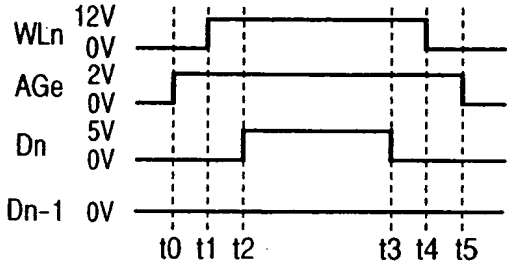


FIG. 19E

TIMING 4

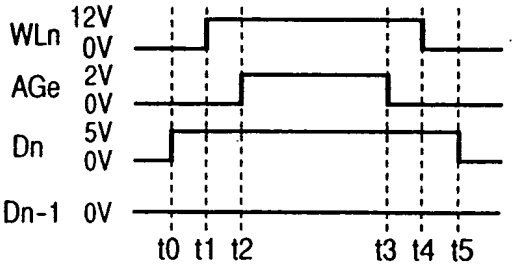


FIG. 19F

TIMING 5

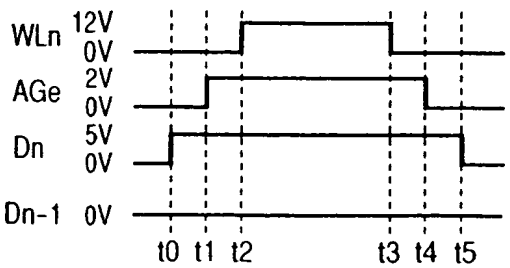


FIG. 19G

TIMING 6

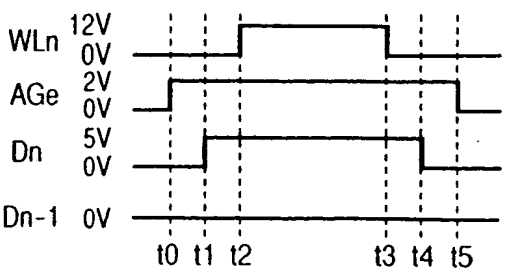


FIG. 20A

ERASE OPERATION VOLTAGE

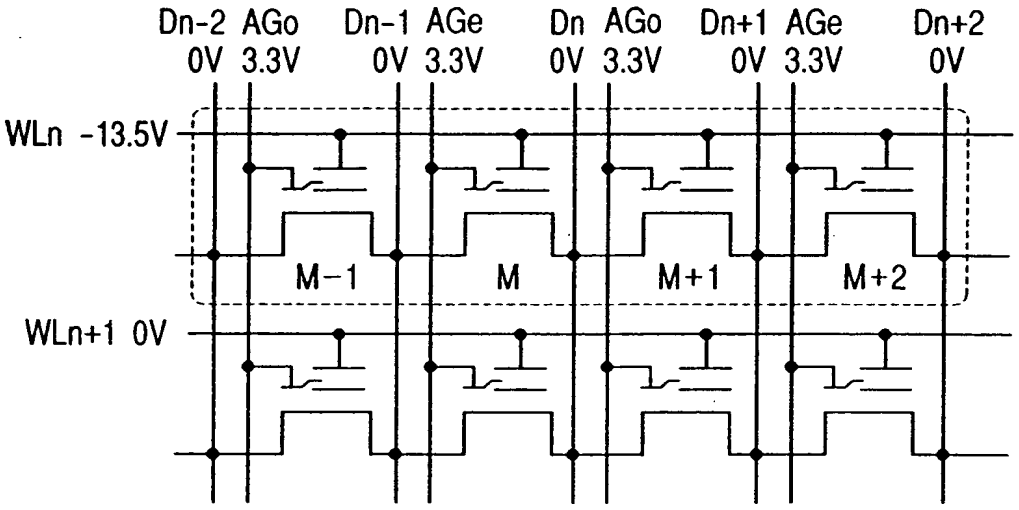


FIG. 20B

TIMING 1

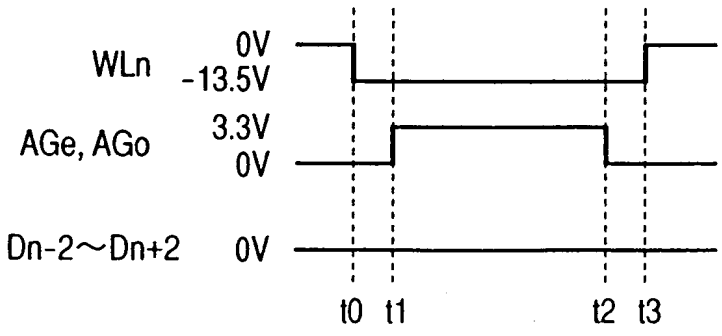


FIG. 21A

READ OPERATION VOLTAGE

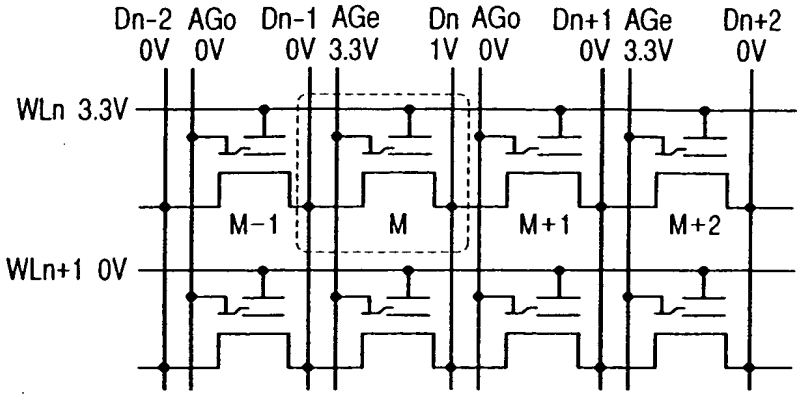


FIG. 21B

TIMING 1

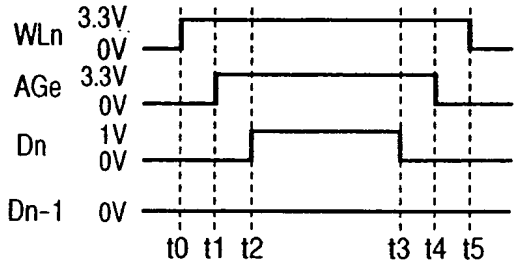


FIG. 21C

TIMING 2

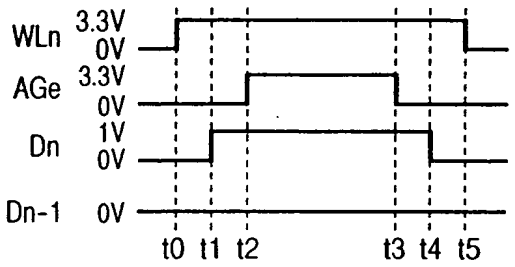


FIG. 21D

TIMING 3

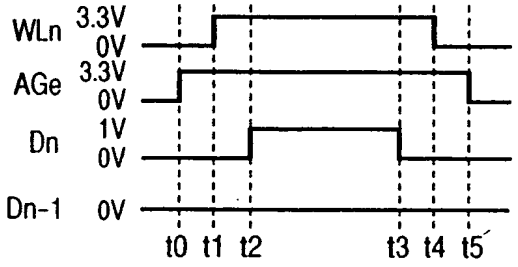


FIG. 21E

TIMING 4

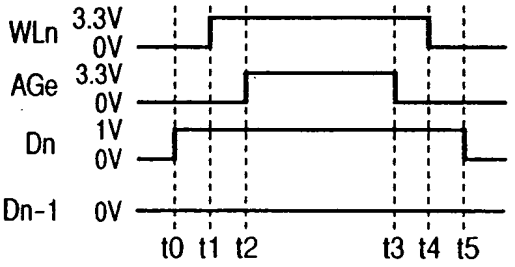


FIG. 21F

TIMING 5

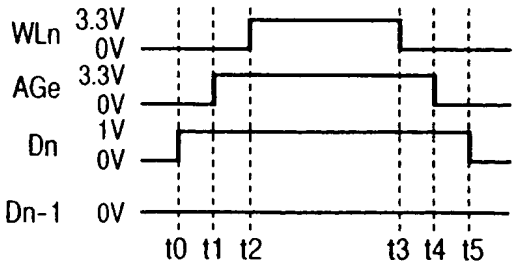


FIG. 21G

TIMING 6

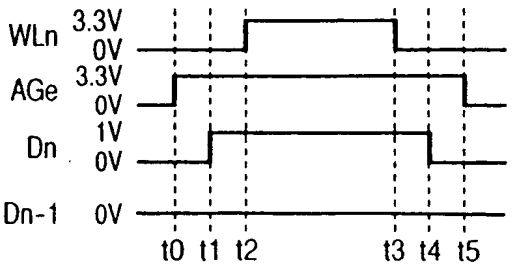


FIG. 22

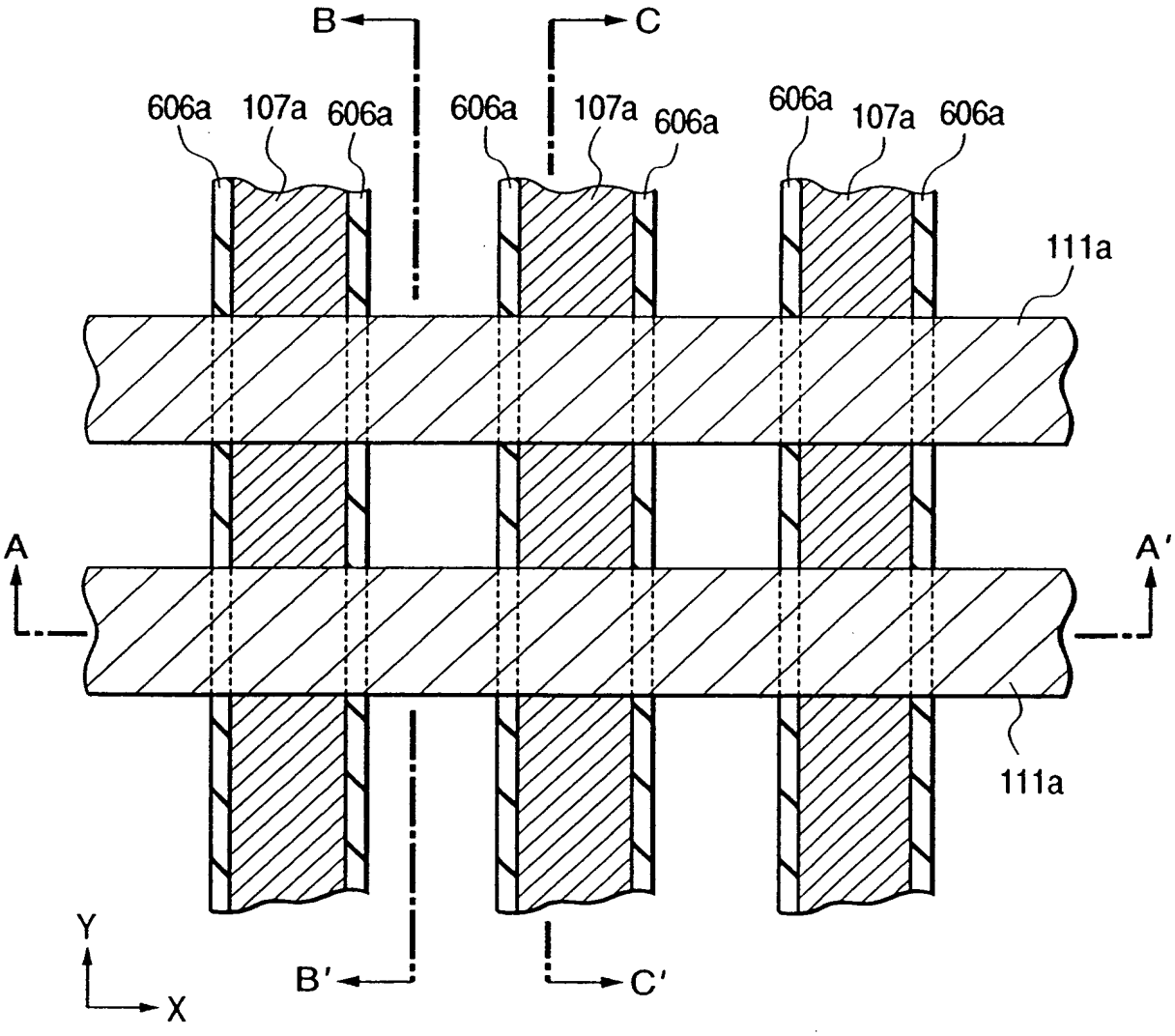

B
C
606a
107a
606a
606a
107a
606a
606a
107a
606a
111a
A
A'
111a
Y
X
B'
C'

FIG. 23A

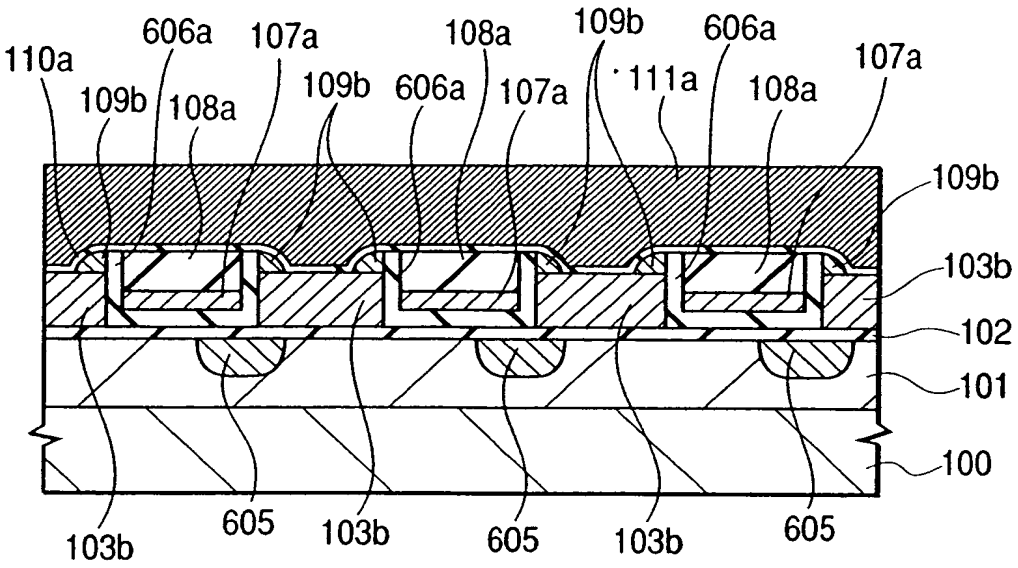


FIG. 23B

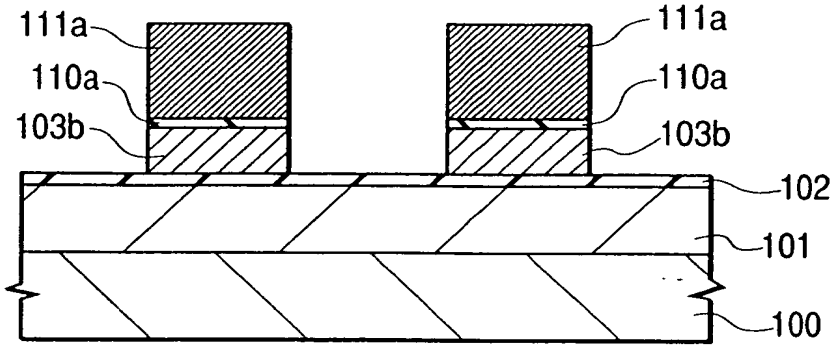


FIG. 23C

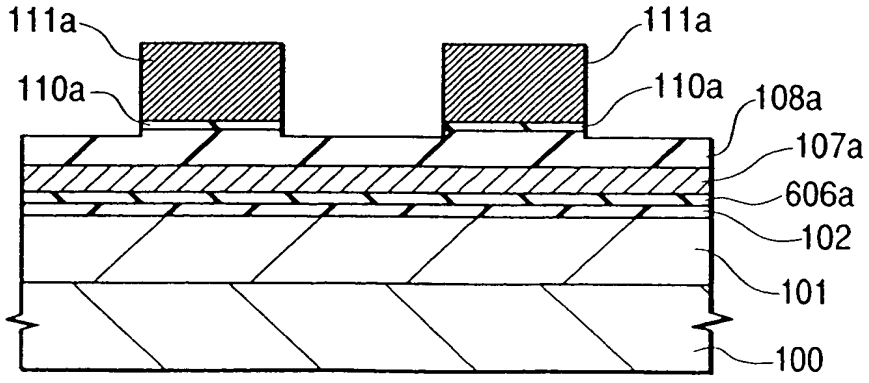


FIG. 24A

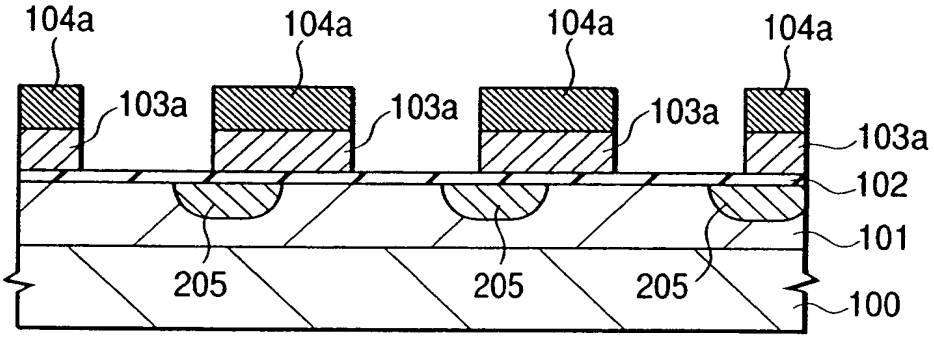


FIG. 24B

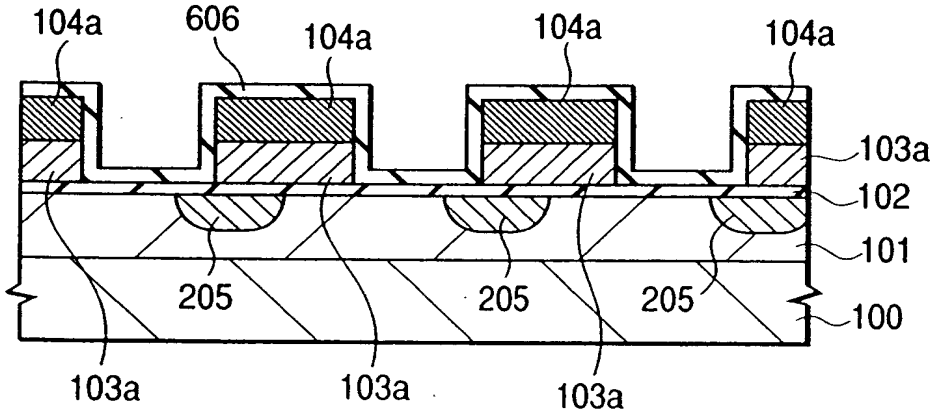


FIG. 25

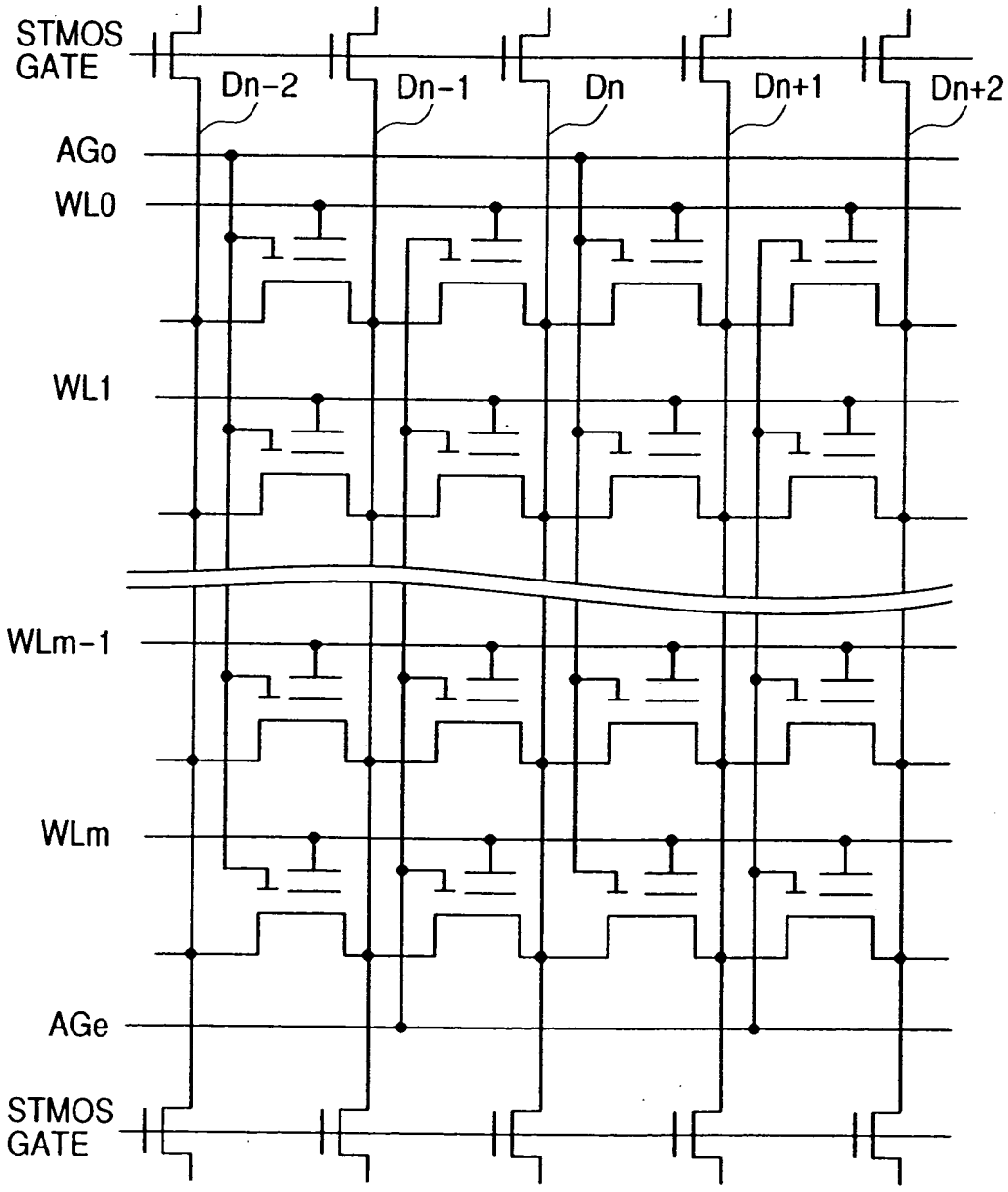

STMOS GATE
Dn-2
Dn-1
Dn
Dn+1
Dn+2
AGo
WL0
WL1
WLm-1
WLm
AGe
STMOS GATE

FIG. 26A

ERASE OPERATION VOLTAGE

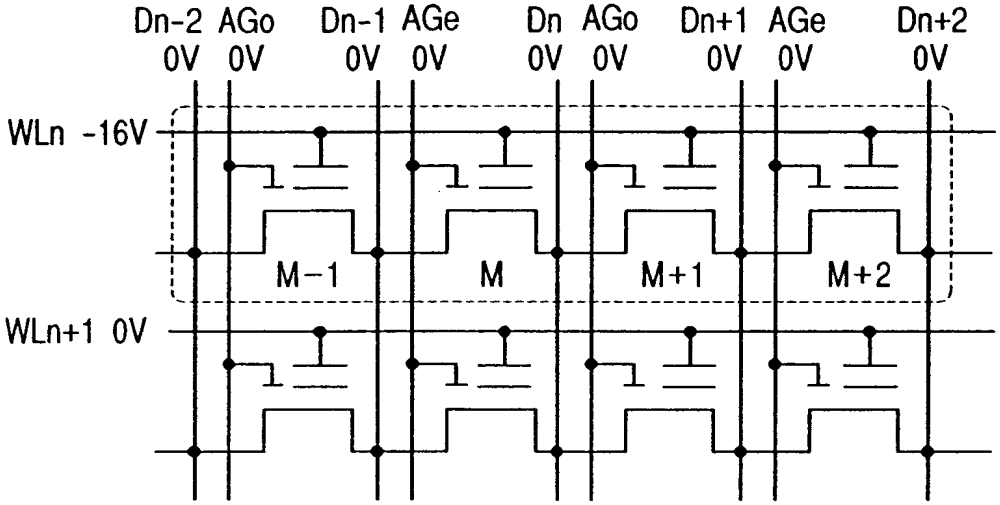


FIG. 26B

TIMING 1

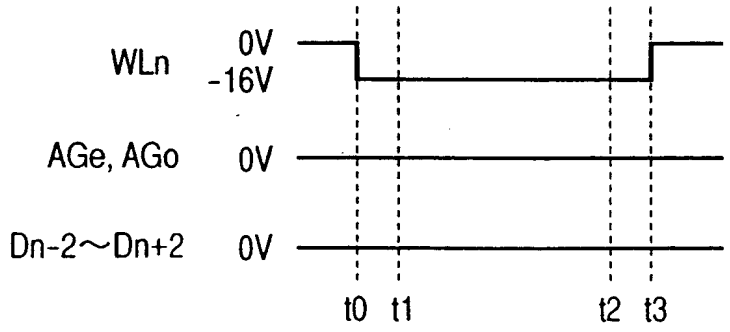


FIG. 27A

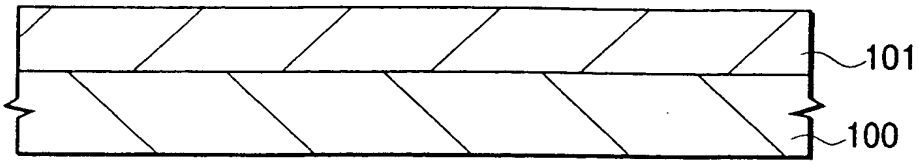


FIG. 27B

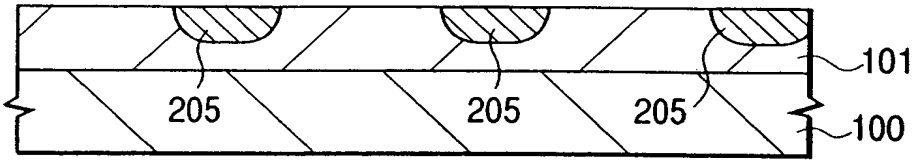


FIG. 27C

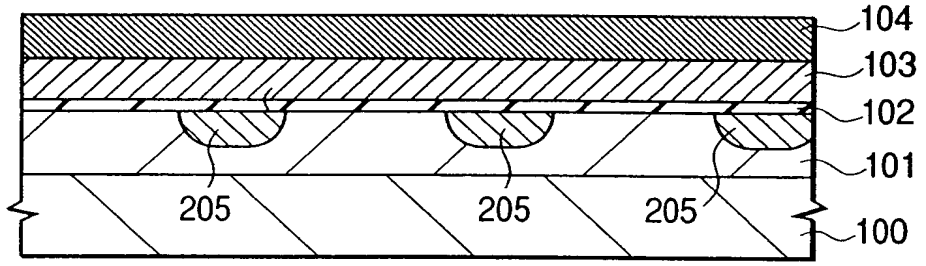


FIG. 27D

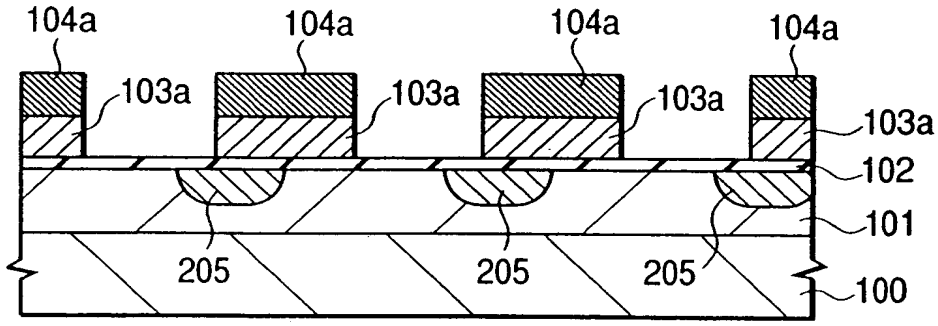


FIG. 27E

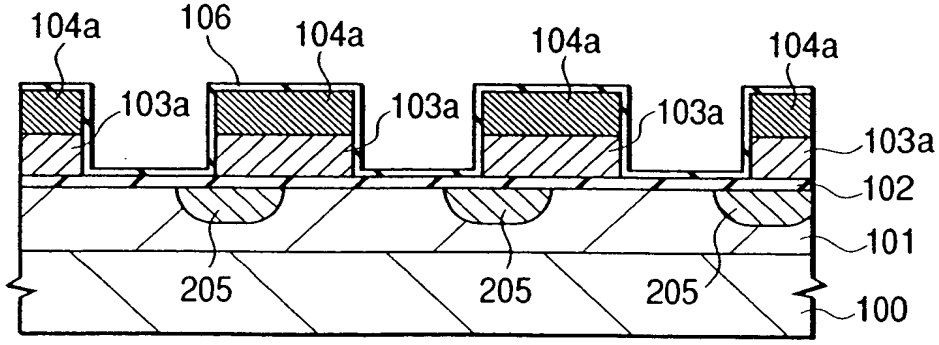


FIG. 28

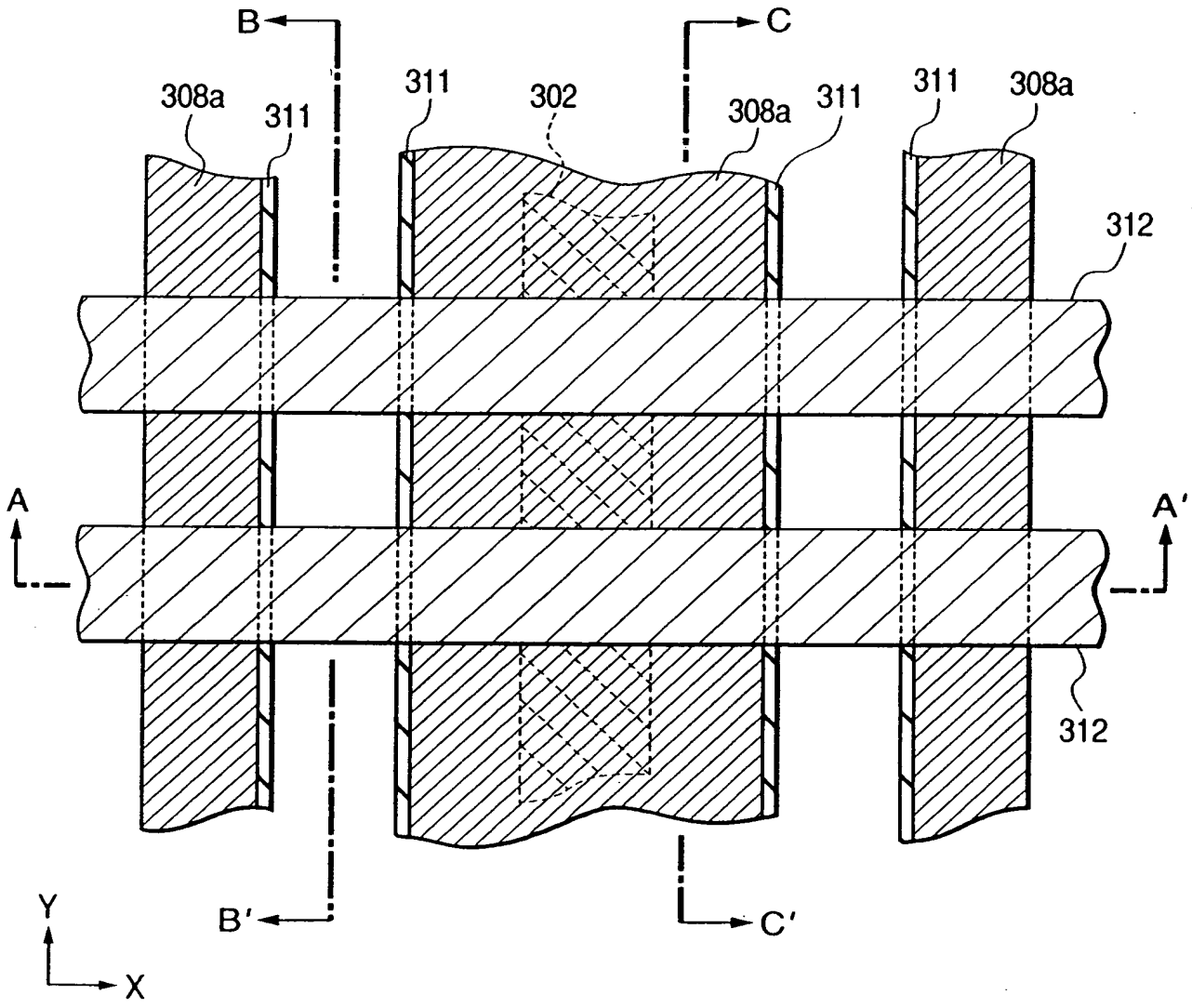


FIG. 29A

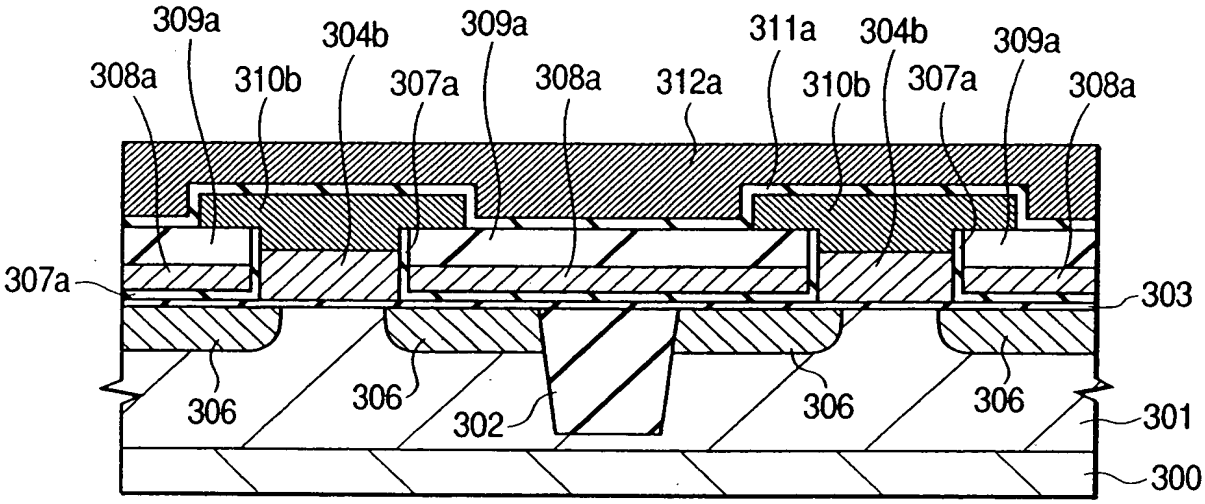


FIG. 29B

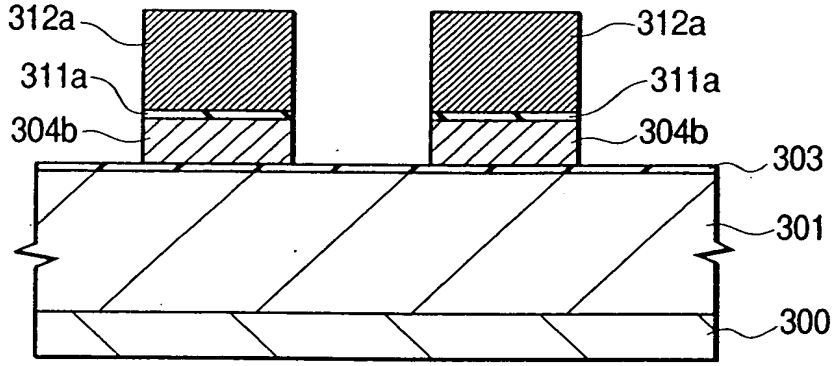


FIG. 29C

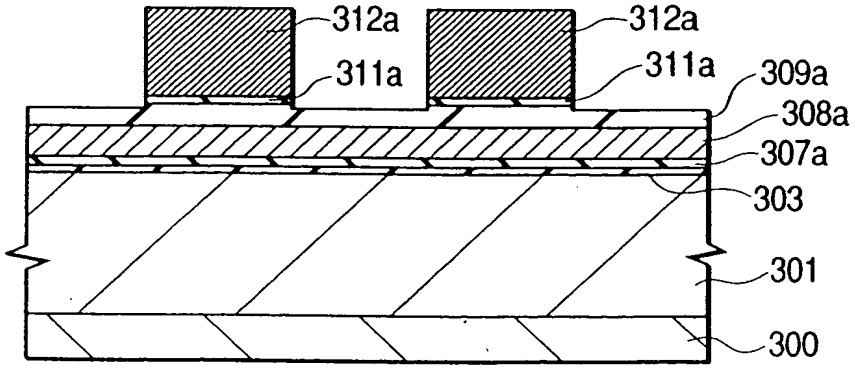


FIG. 30A

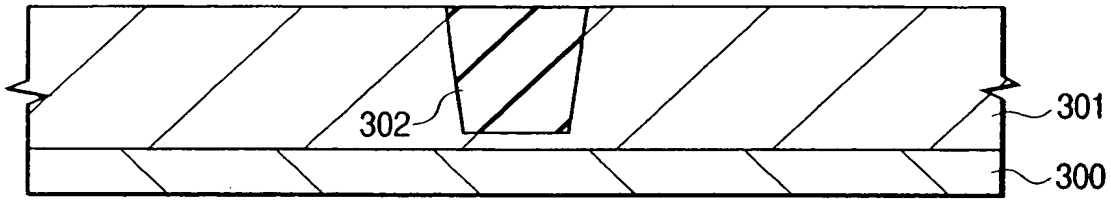


FIG. 30B

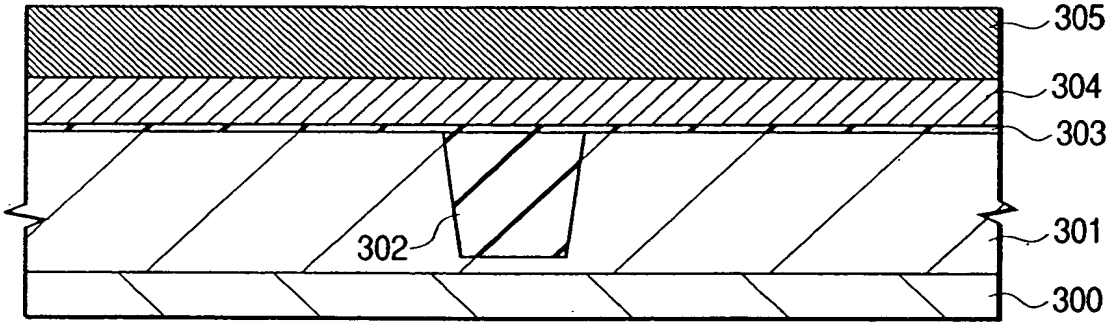


FIG. 30C

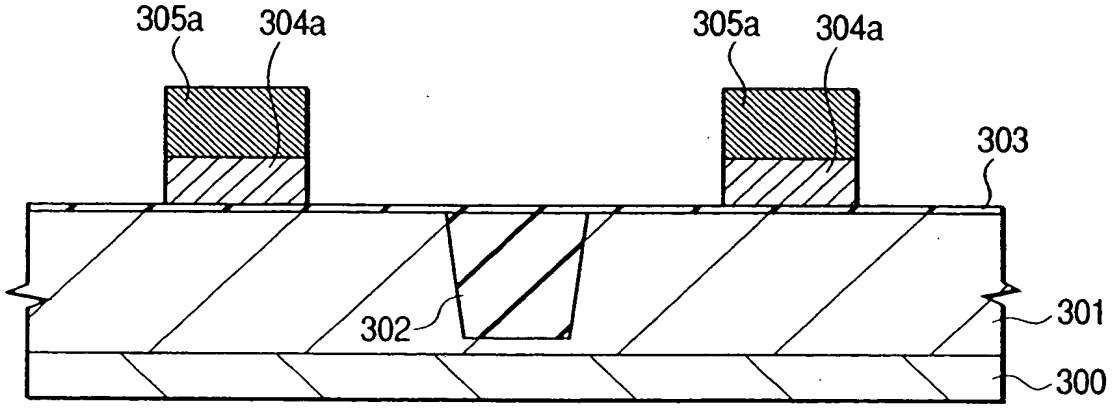


FIG. 31A

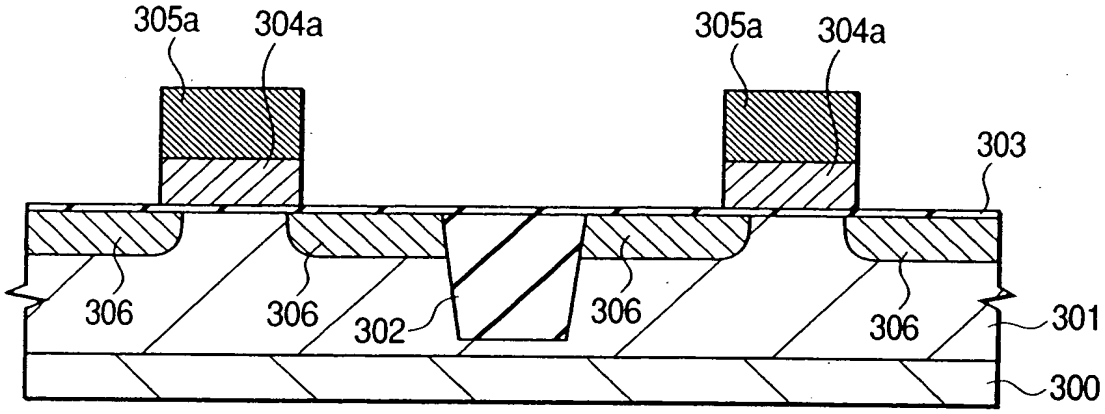


FIG. 31B

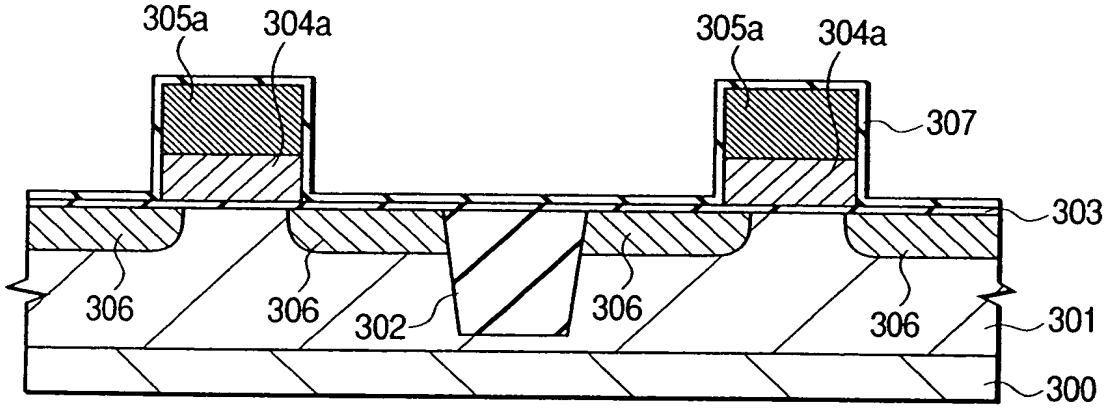


FIG. 31C

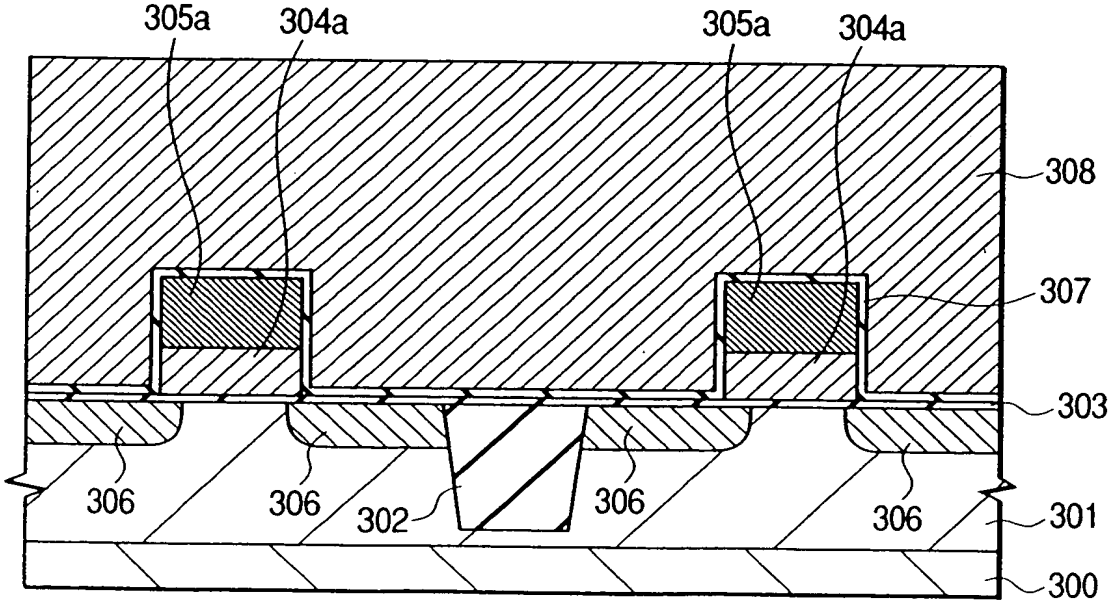


FIG. 32A

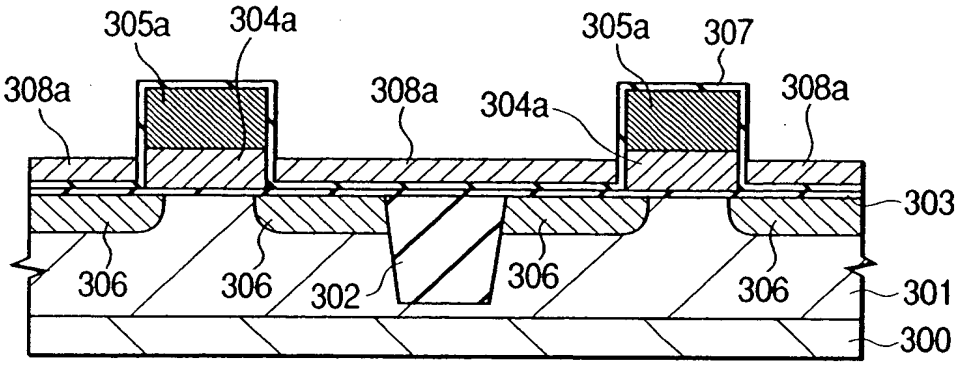


FIG. 32B

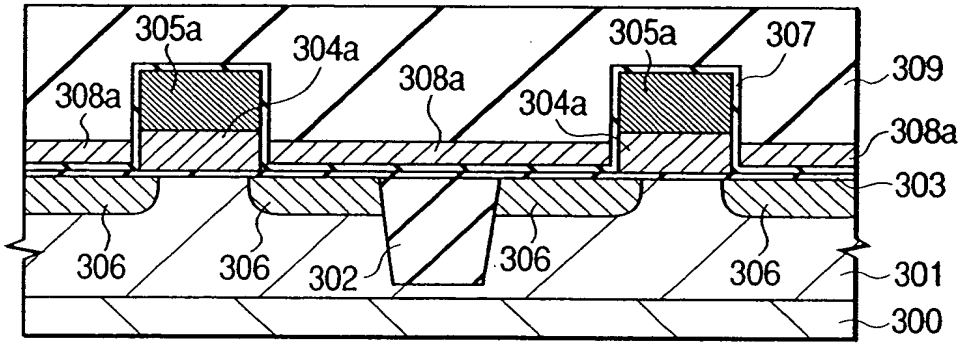


FIG. 32C

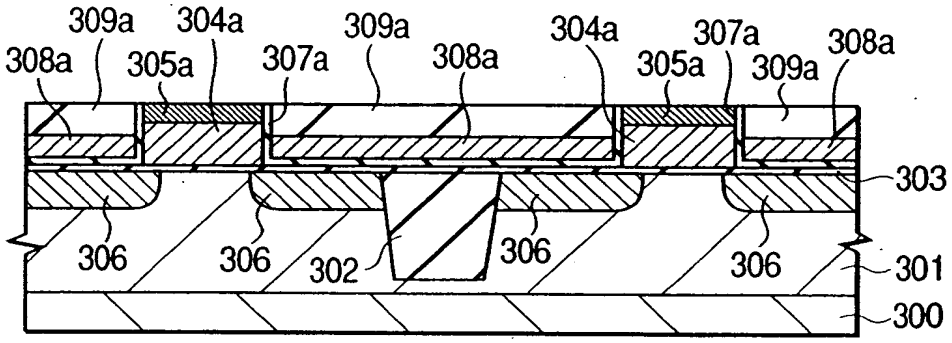


FIG. 32D

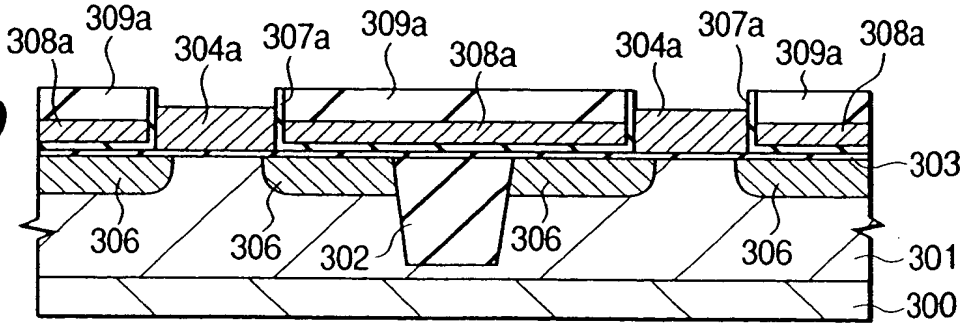


FIG. 33A

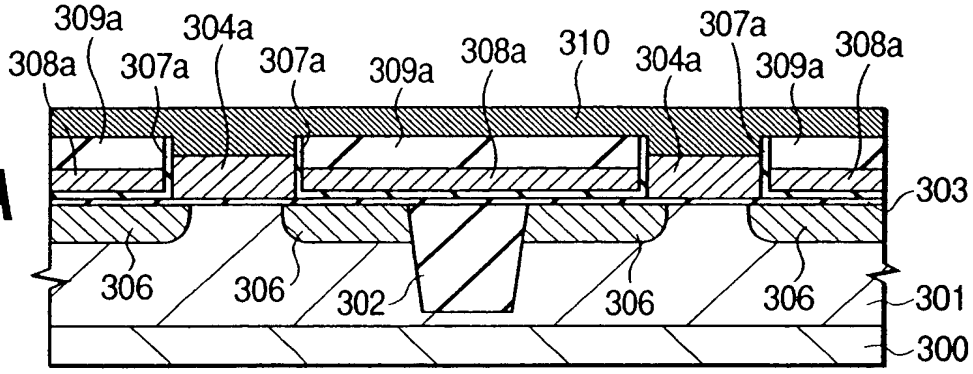


FIG. 33B

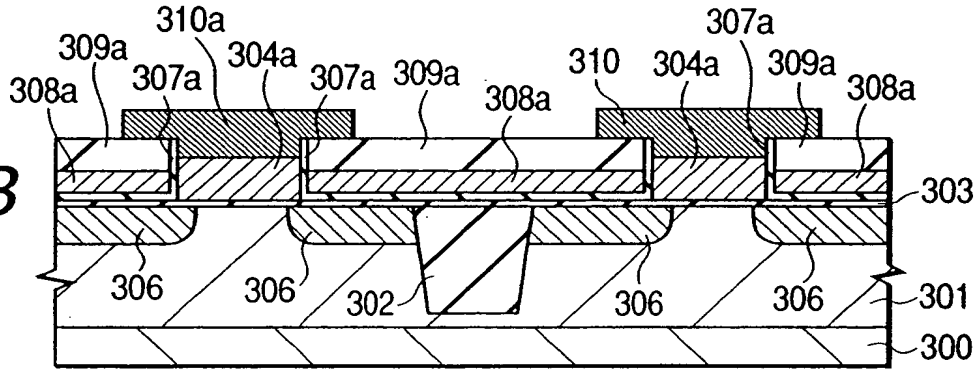


FIG. 33C

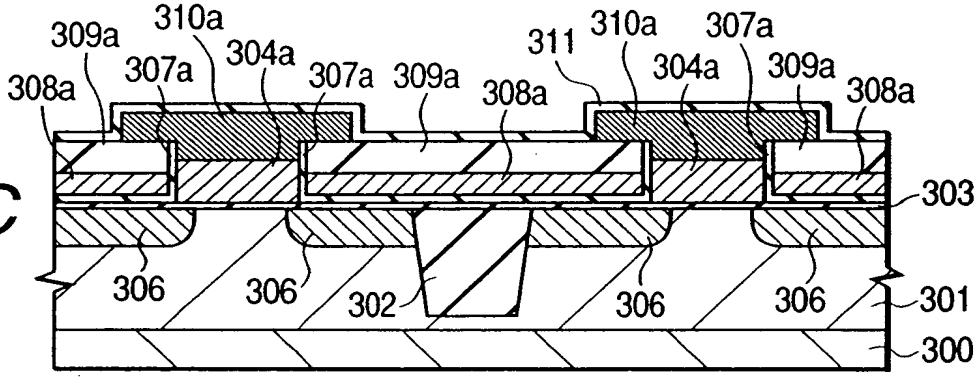


FIG. 33D

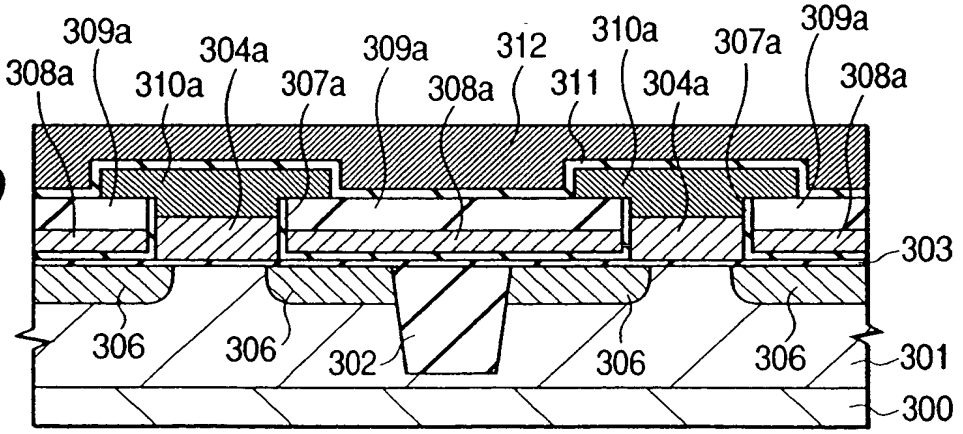


FIG. 34

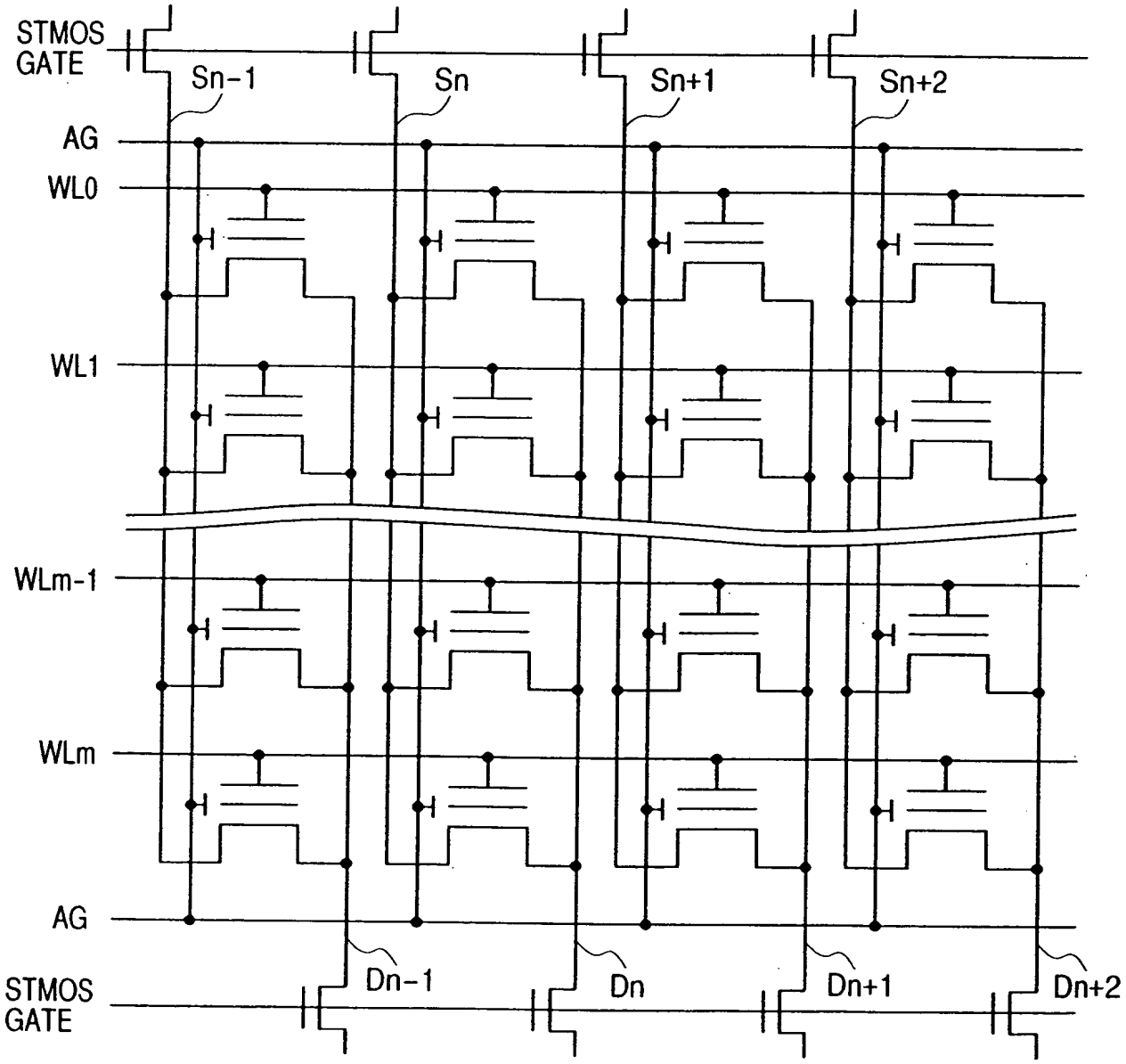

STMOS GATE
Sn-1
Sn
Sn+1
Sn+2
AG
WL0
WL1
WLm-1
WLm
AG
STMOS GATE
Dn-1
Dn
Dn+1
Dn+2

FIG. 35A

PROGRAM OPERATION VOLTAGE

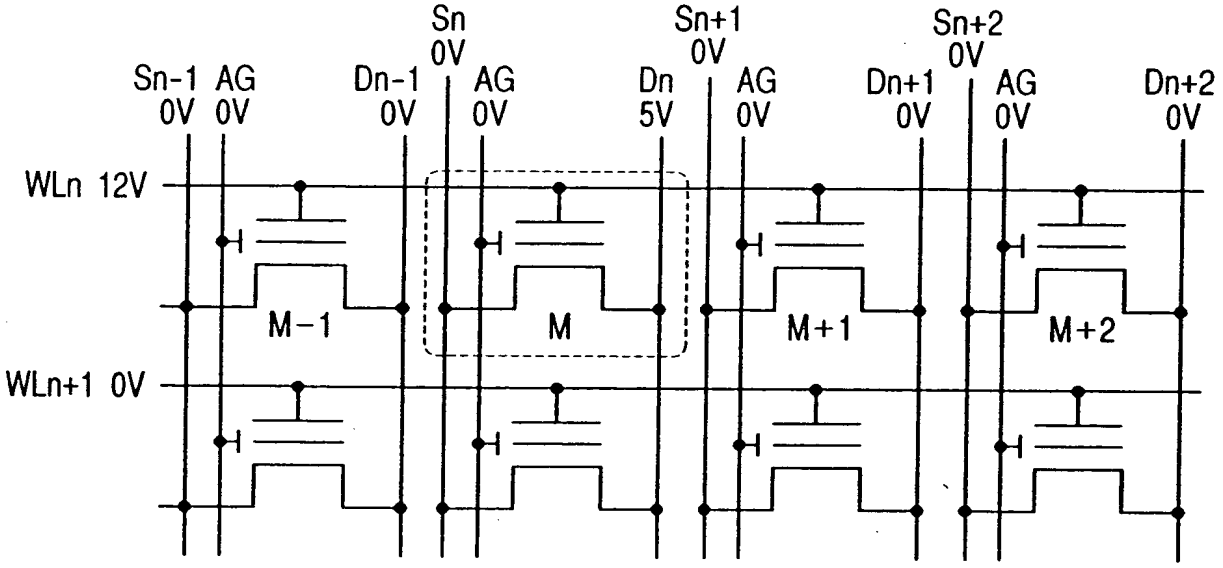


FIG. 35B

TIMING 1

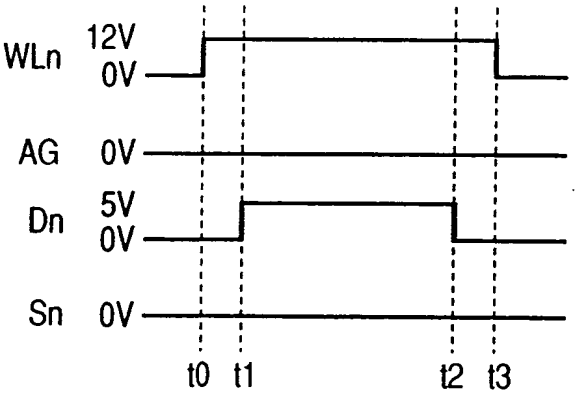


FIG. 35C

TIMING 2

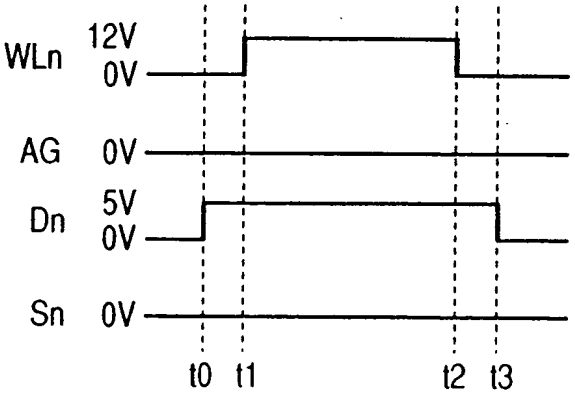


FIG. 36A

ERASE OPERATION VOLTAGE

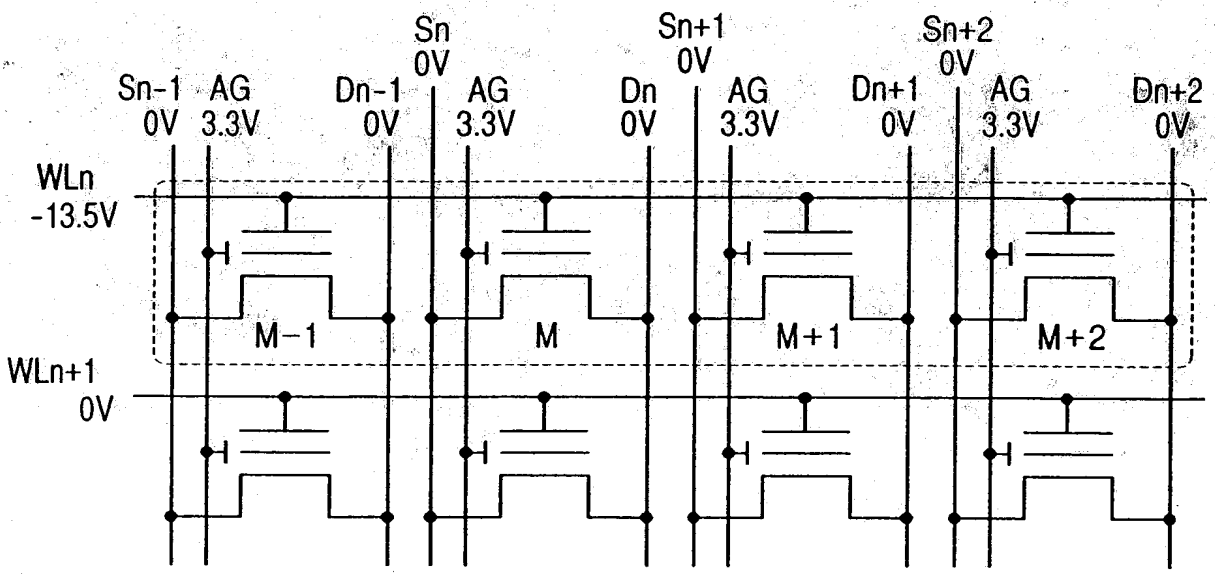


FIG. 36B

TIMING 1

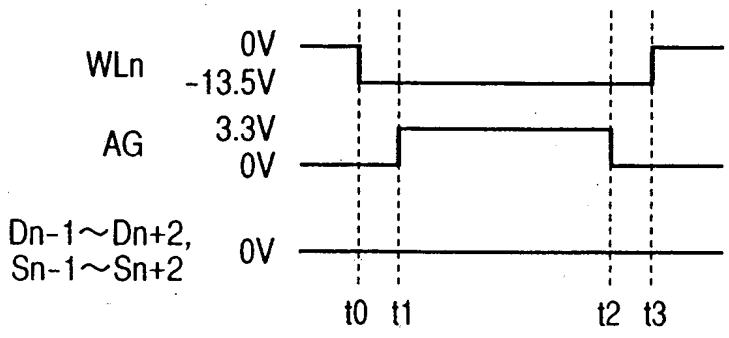


FIG. 37A

READ OPERATION VOLTAGE

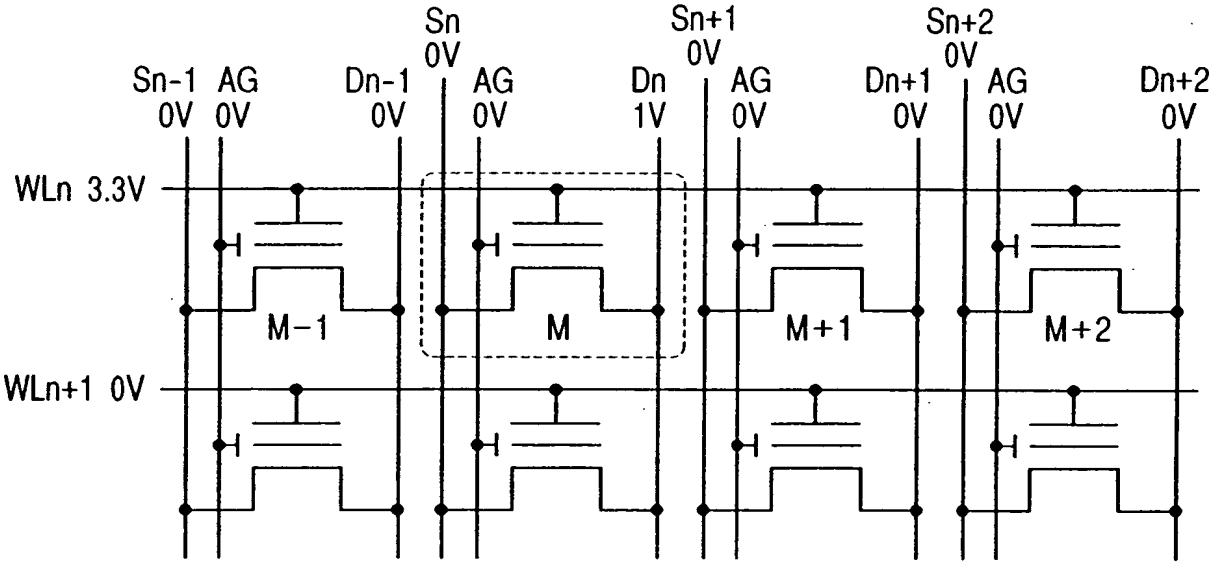


FIG. 37B

TIMING 1

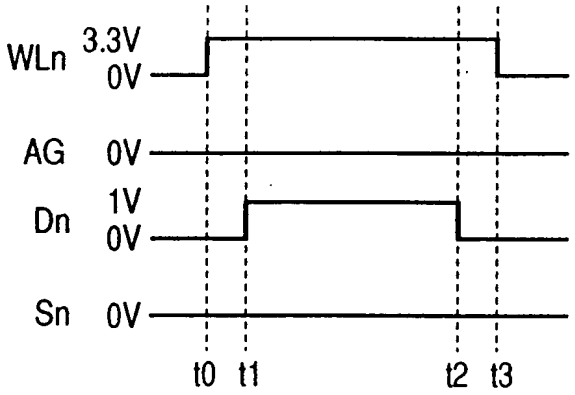


FIG. 37C

TIMING 2

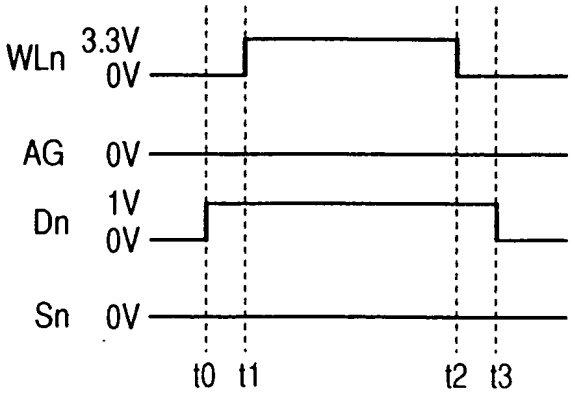


FIG. 38

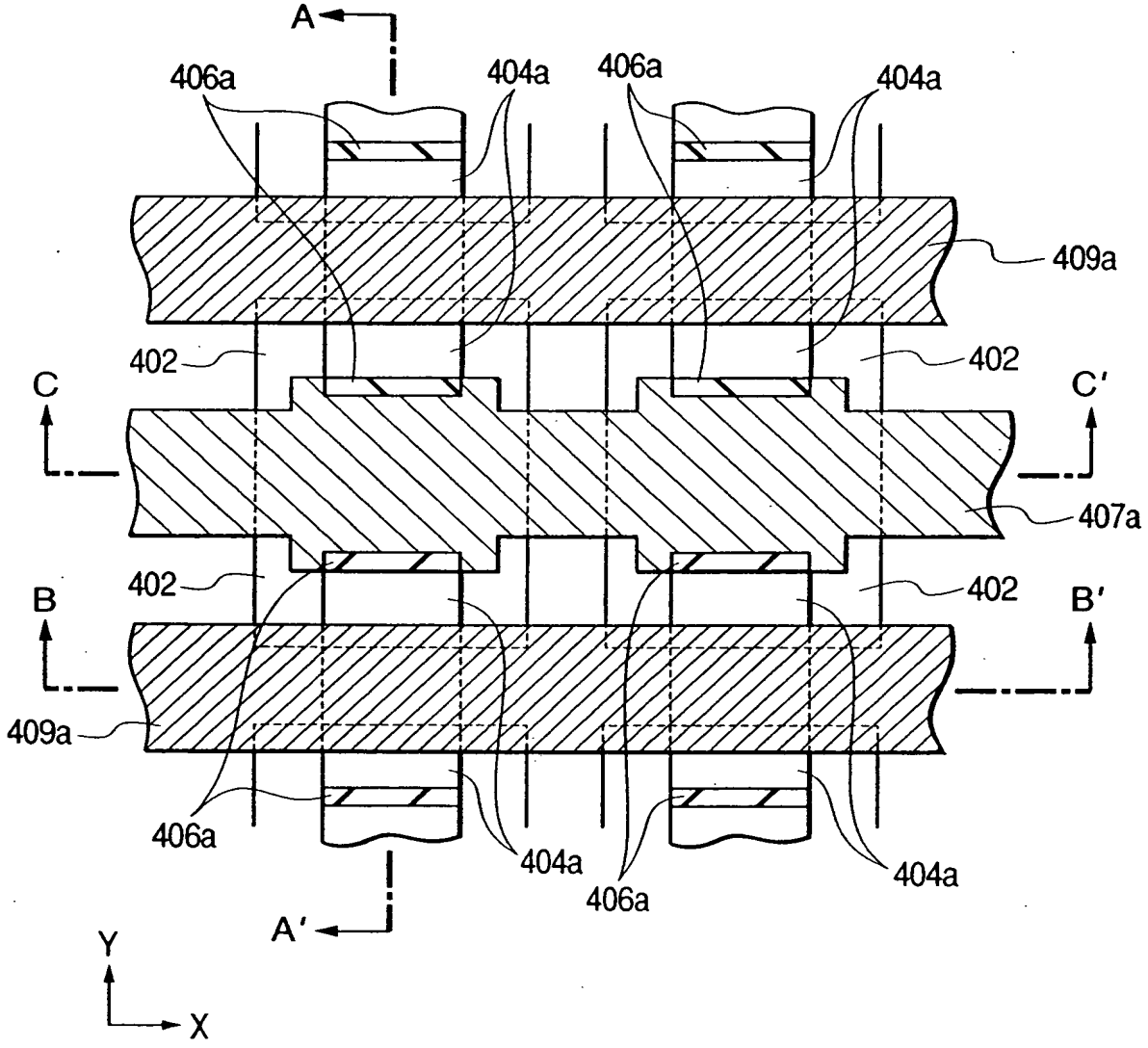

A
406a
404a
406a
404a
409a
402
402
C
C'
407a
402
402
B
B'
409a
406a
404a
406a
404a
A'
Y
X

FIG. 39A

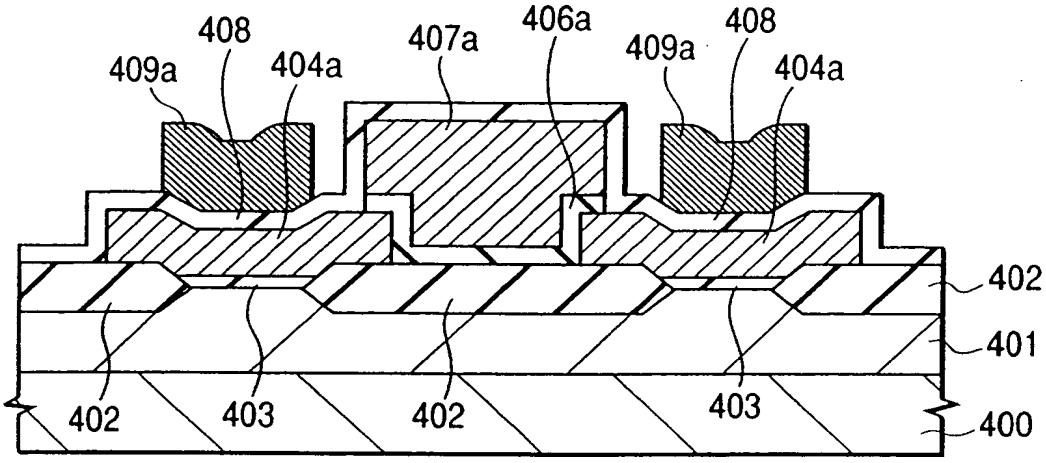


FIG. 39B

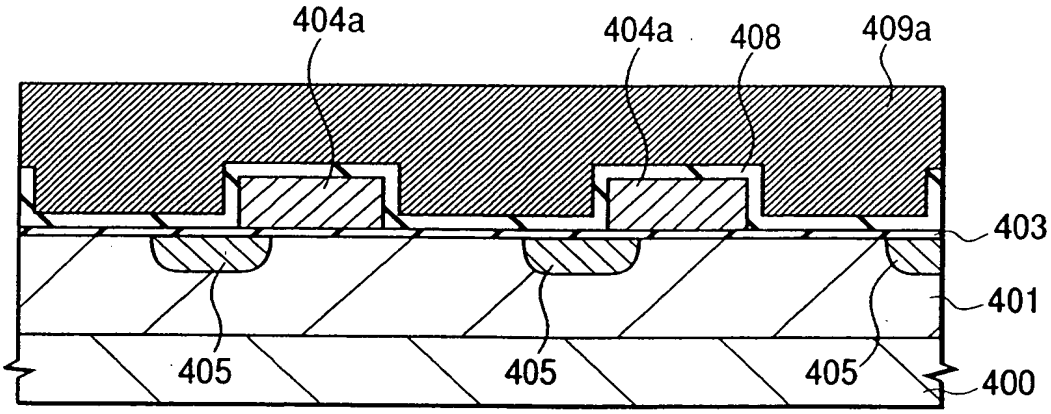


FIG. 39C

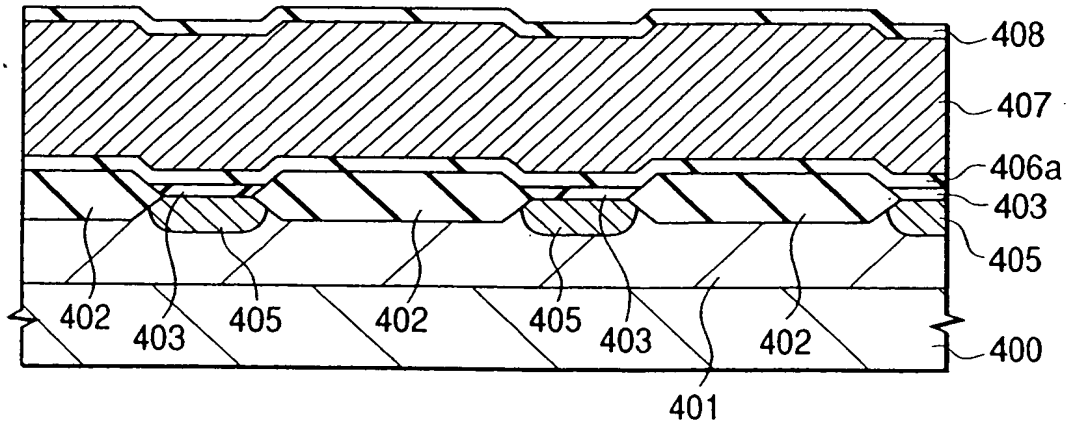


FIG. 40A

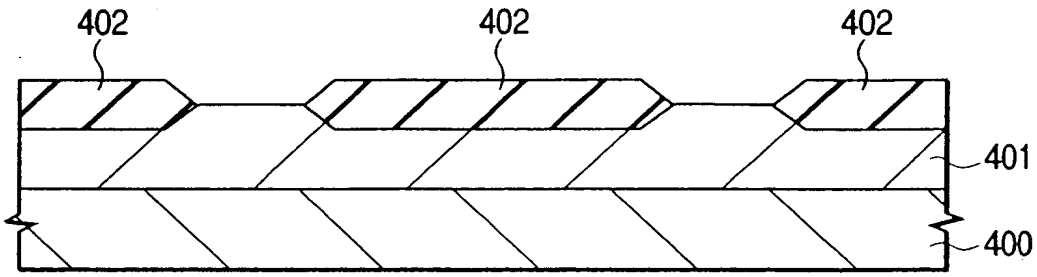


FIG. 40B

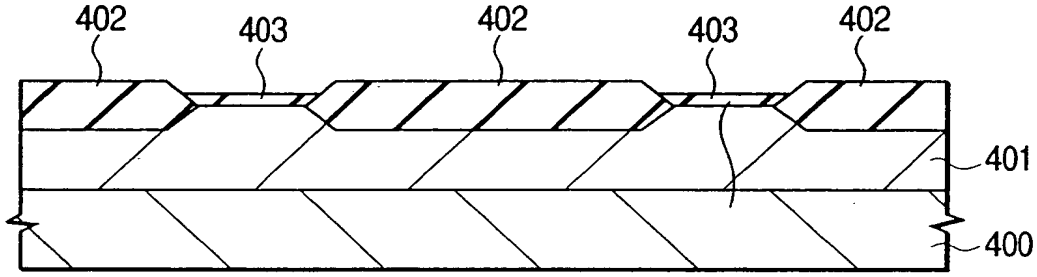


FIG. 40C

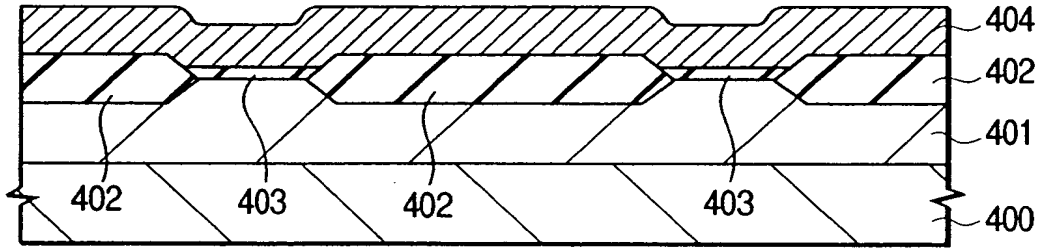


FIG. 40D

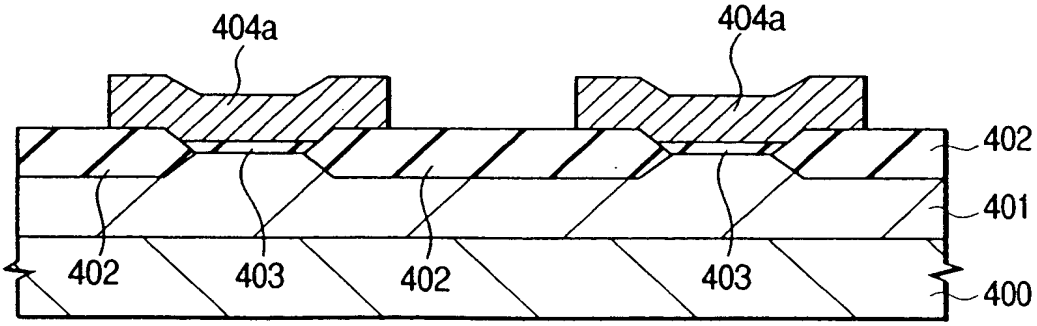


FIG. 41A

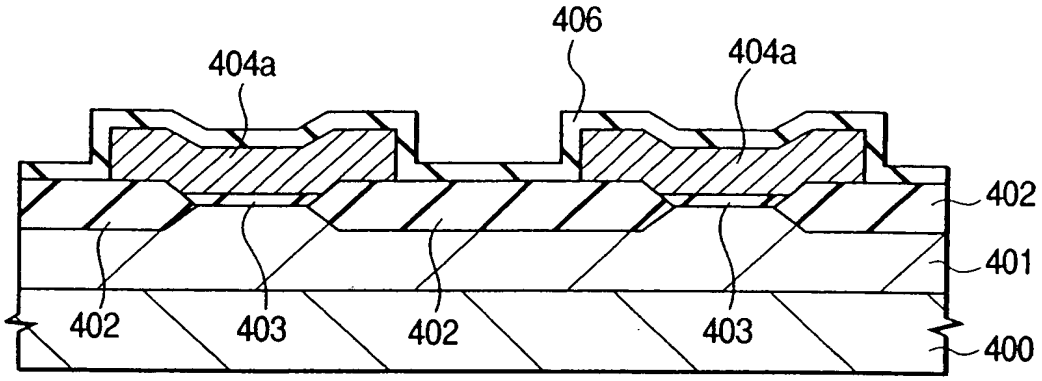


FIG. 41B

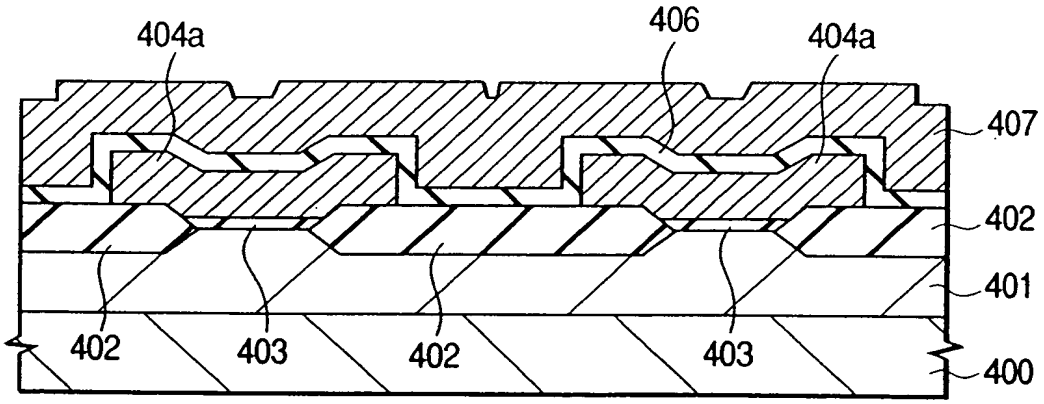


FIG. 41C

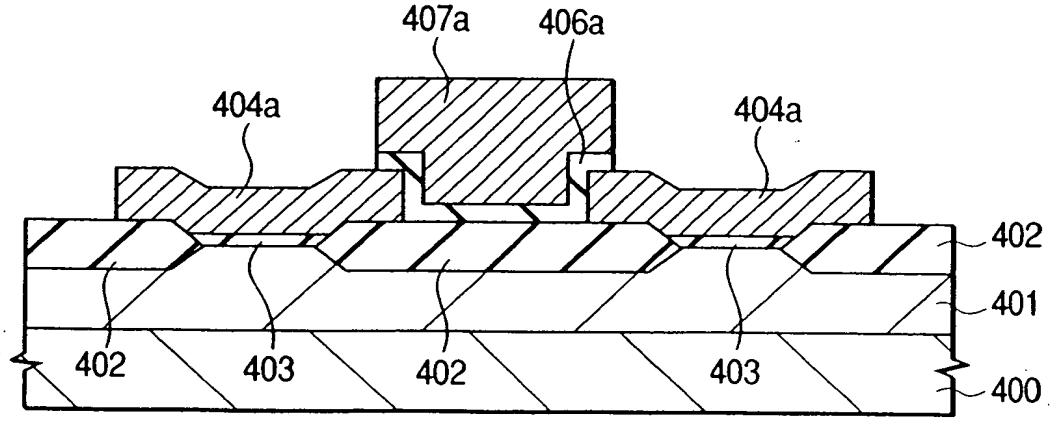


FIG. 42A

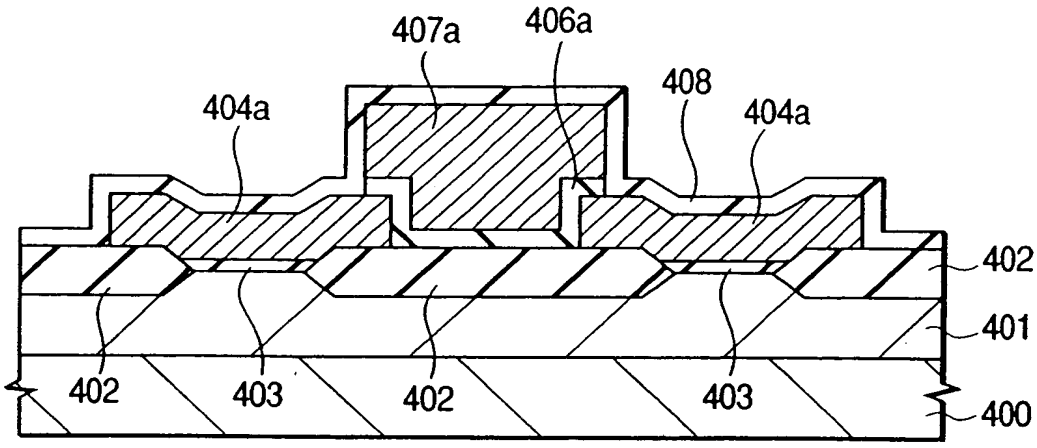


FIG. 42B

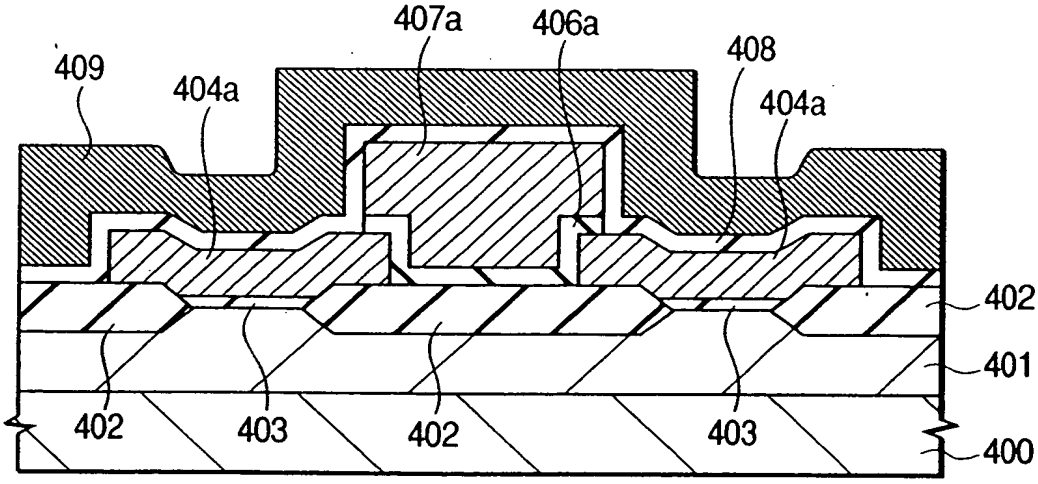


FIG. 42C

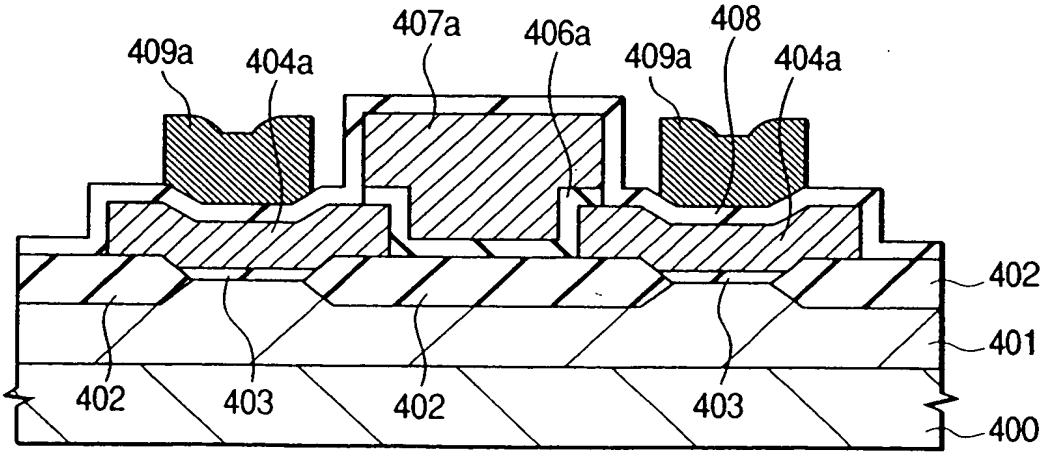


FIG. 43A

PROGRAM OPERATION VOLTAGE

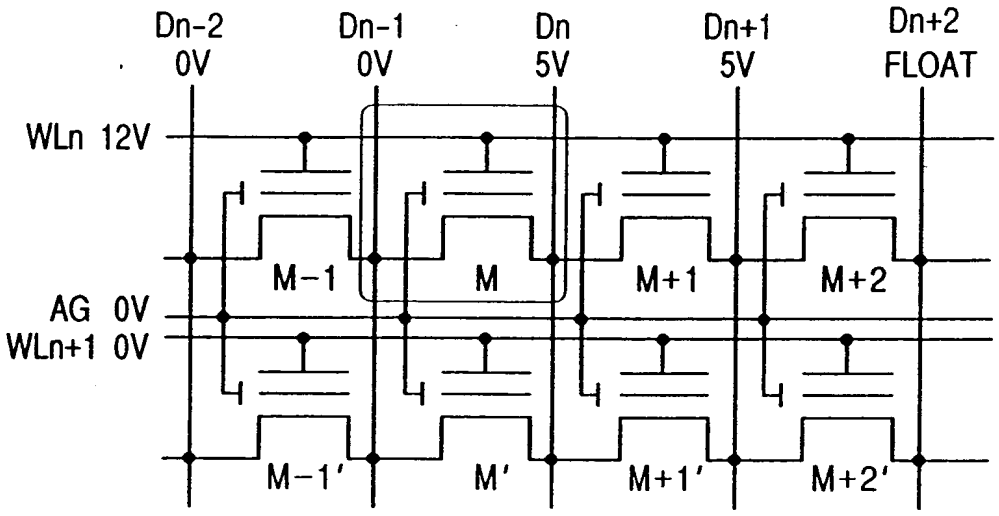


FIG. 43B

TIMING 1

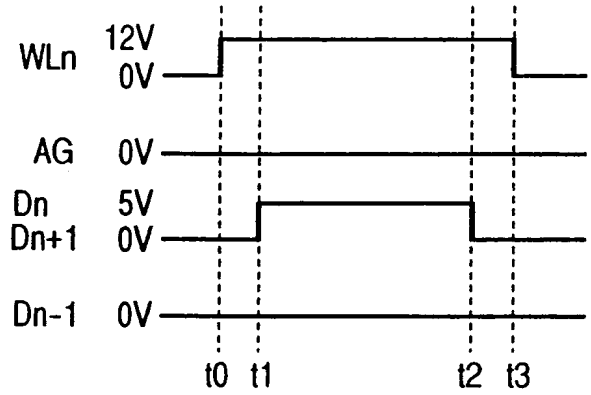


FIG. 43C

TIMING 2

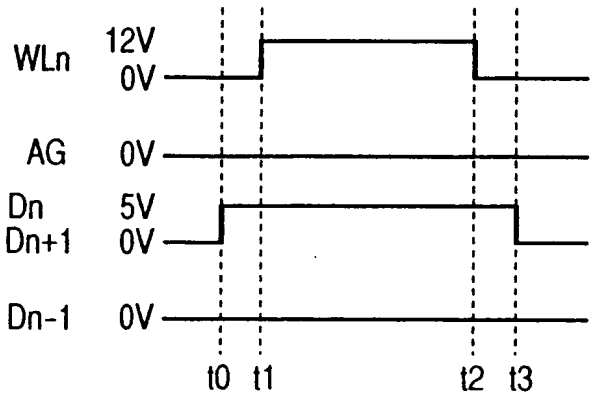


FIG. 44A

ERASE OPERATION VOLTAGE

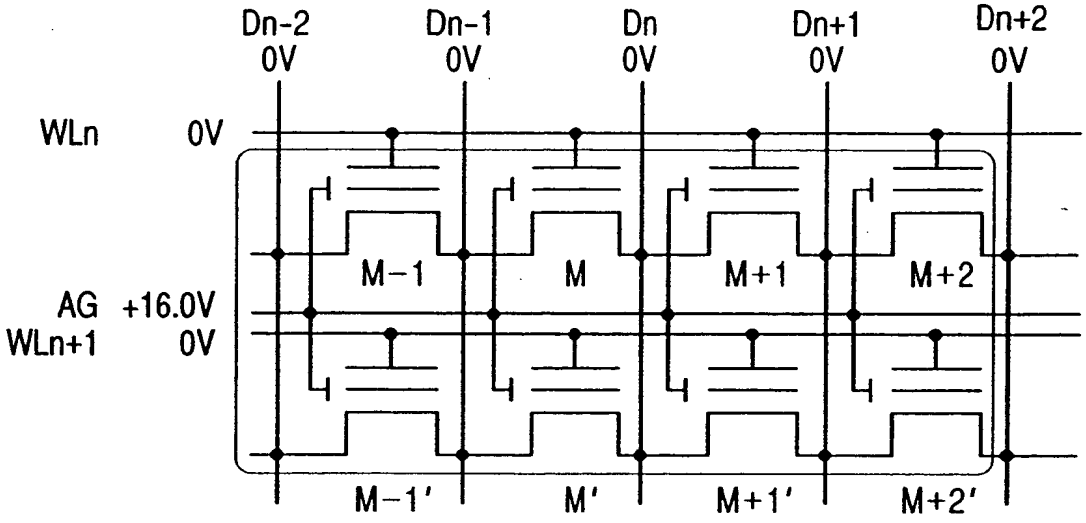


FIG. 44B

ERASE OPERATION VOLTAGE

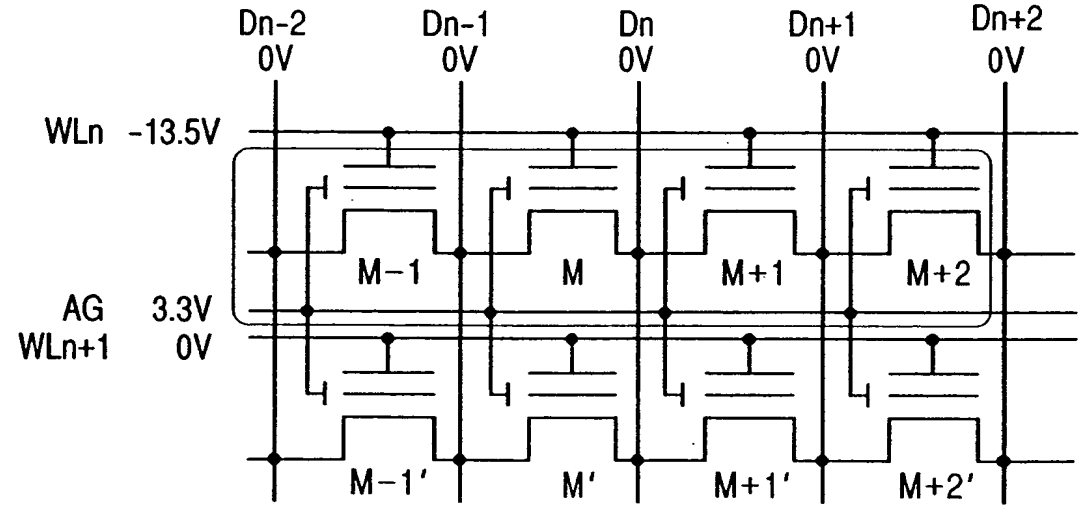


FIG. 44C

TIMING 1

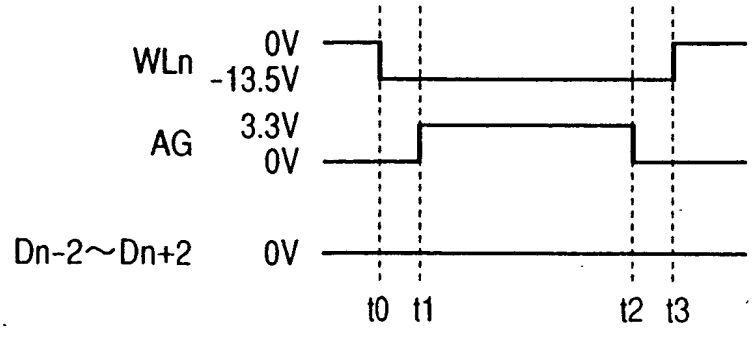


FIG. 45A

READ OPERATION VOLTAGE

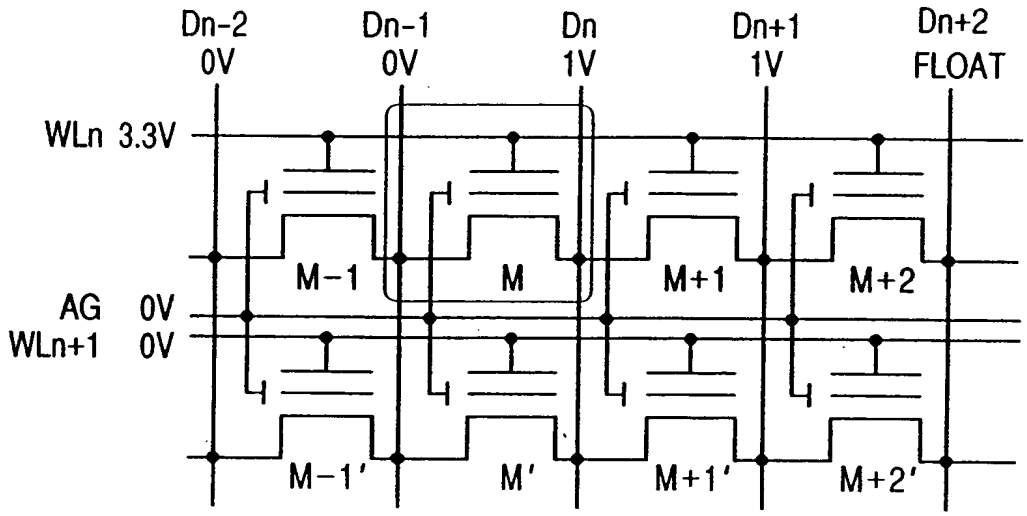


FIG. 45B

TIMING 1

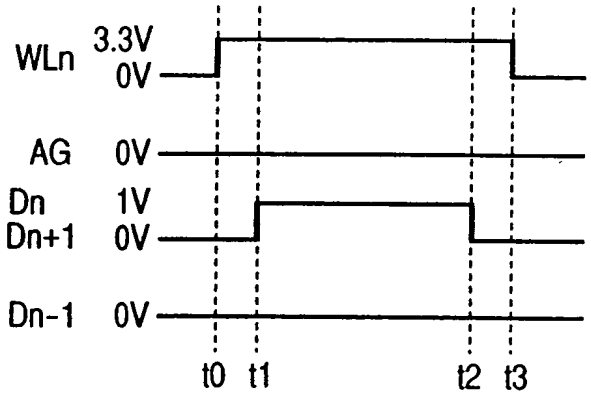


FIG. 45C

TIMING 2

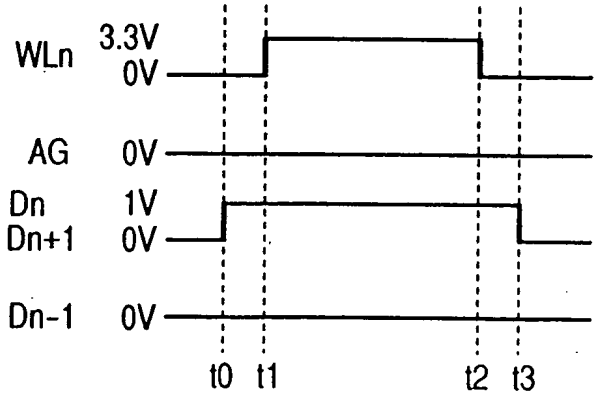


FIG. 46

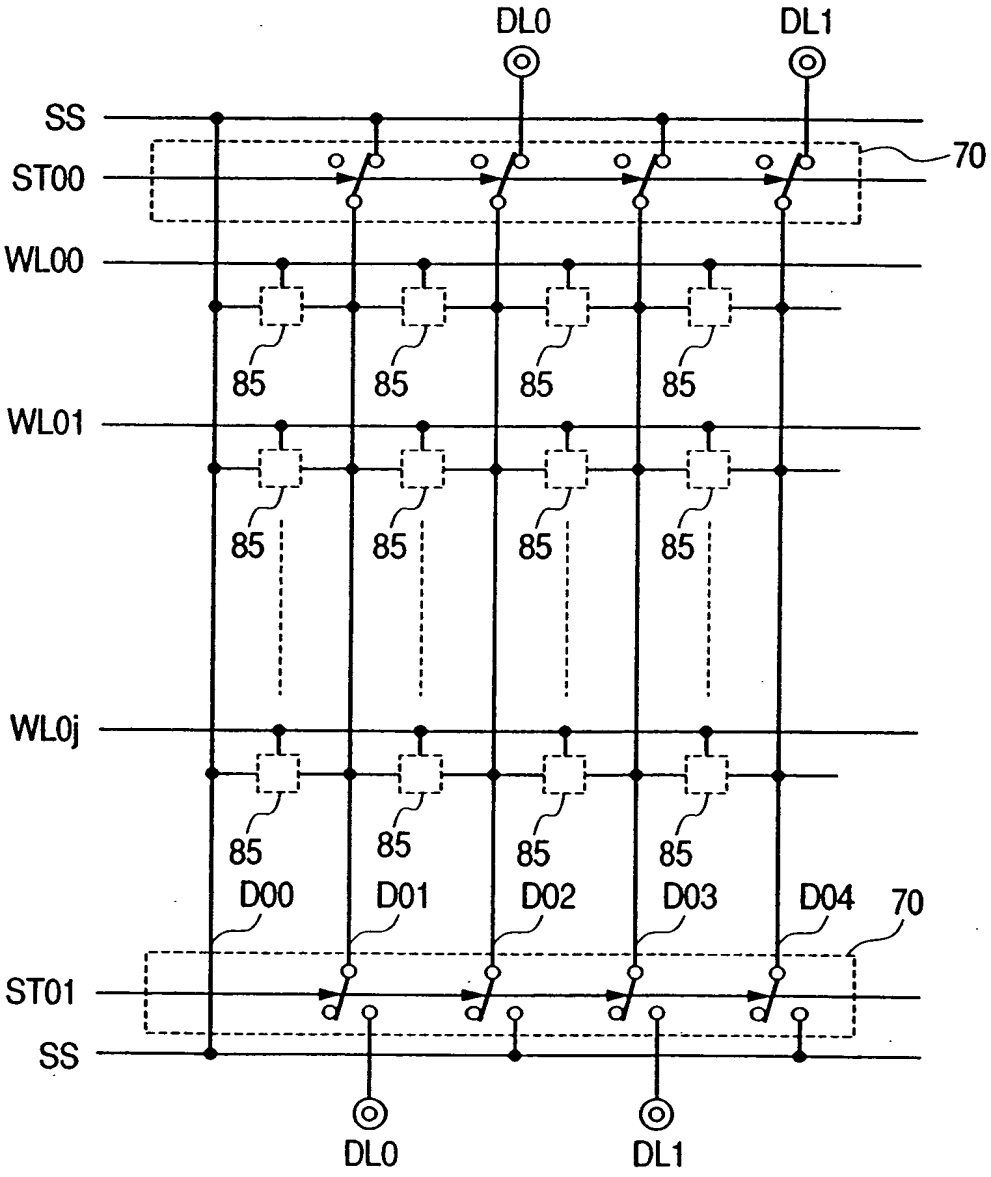

DL0
DL1
SS
ST00
70
WL00
85
WL01
WL0j
D00
D01
D02
D03
D04
ST01
SS
DL0
DL1

FIG. 47

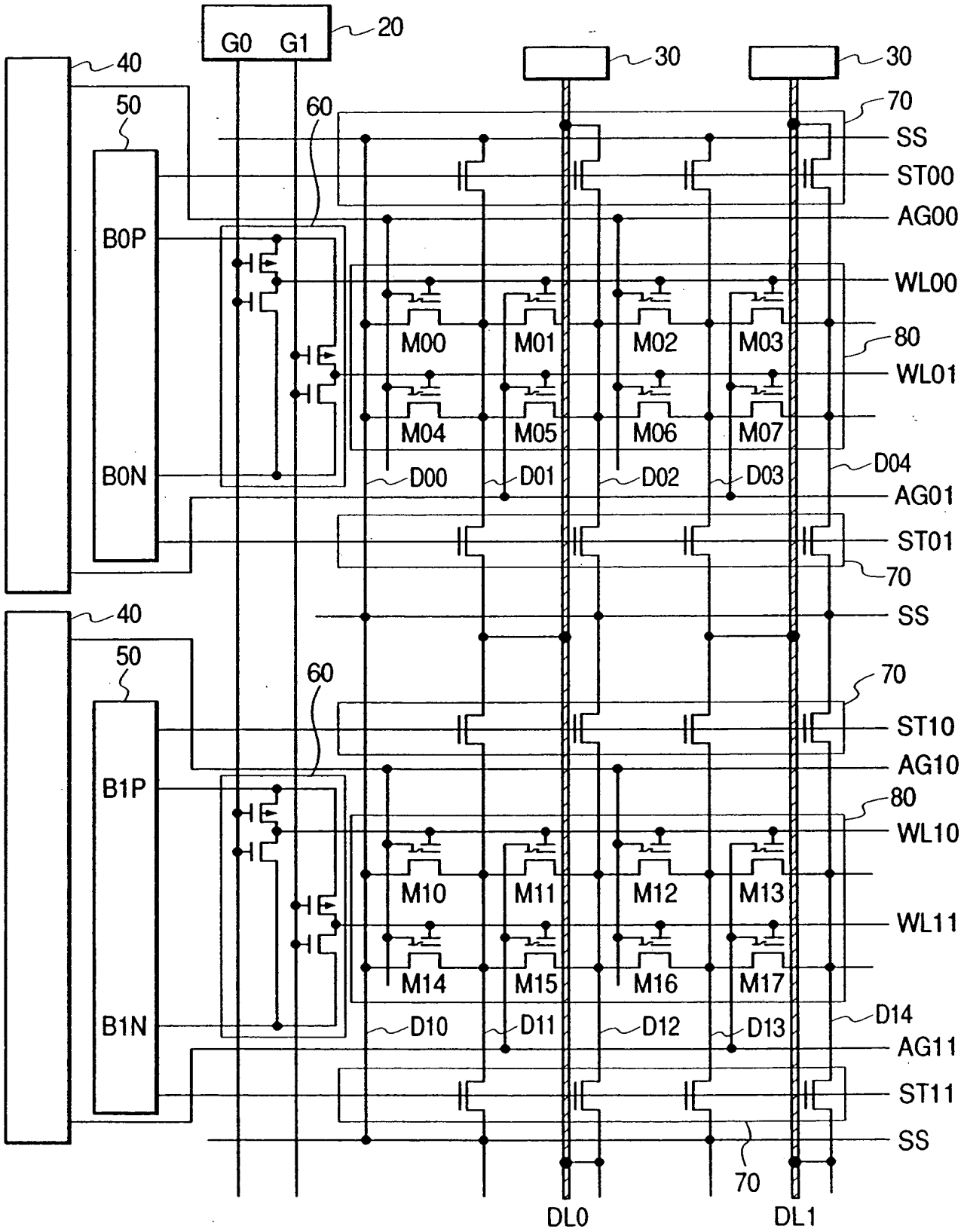

G0
G1
20
30
30
40
50
60
70
SS
ST00
AG00
B0P
WL00
M00
M01
M02
M03
80
WL01
M04
M05
M06
M07
B0N
D00
D01
D02
D03
D04
AG01
ST01
70
40
SS
50
60
70
ST10
AG10
B1P
80
WL10
M10
M11
M12
M13
WL11
M14
M15
M16
M17
B1N
D10
D11
D12
D13
D14
AG11
ST11
SS
70
DL0
DL1

FIG. 48

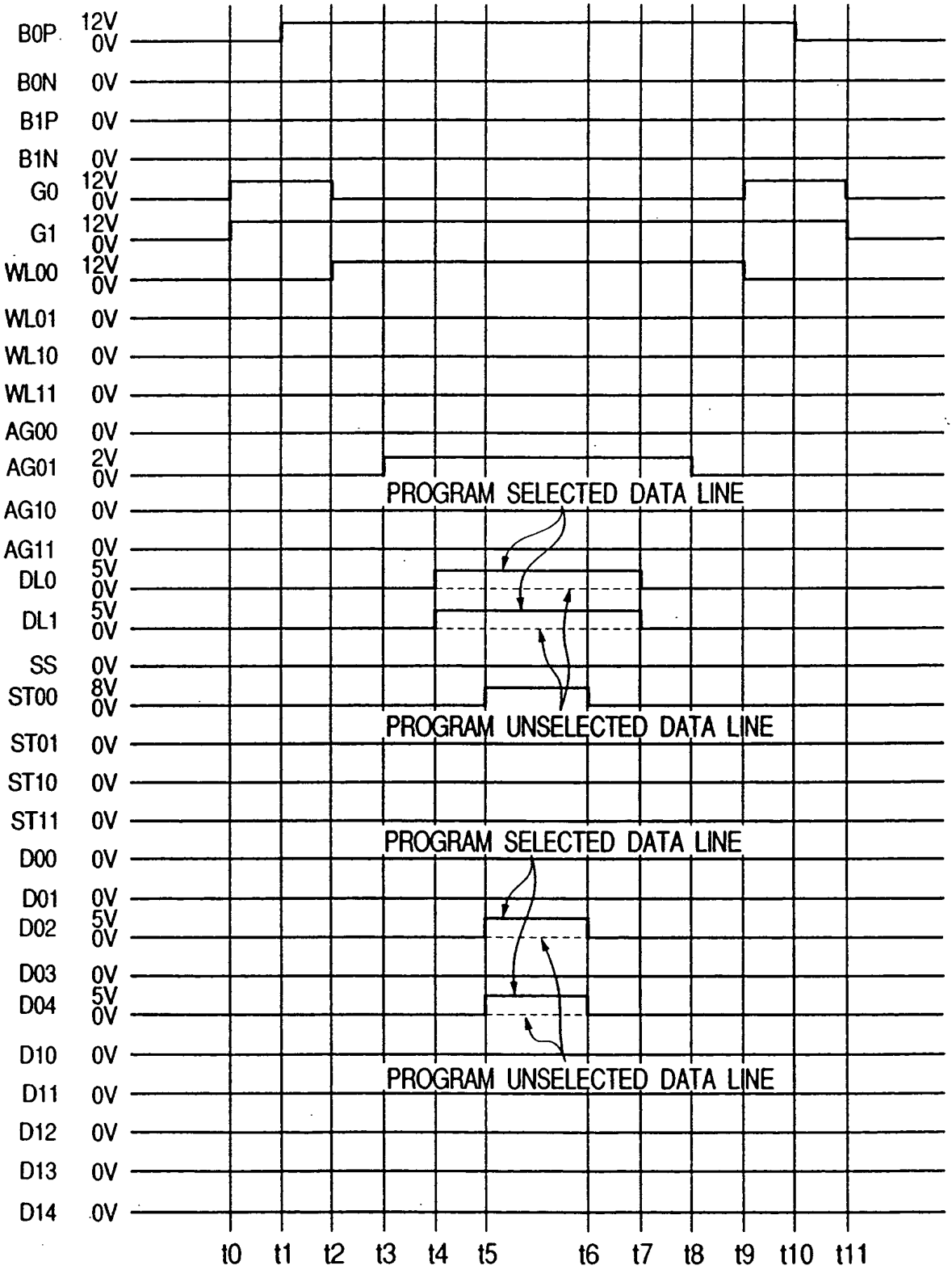

B0P
B0N
B1P
B1N
G0
G1
WL00
WL01
WL10
WL11
AG00
AG01
AG10
AG11
DL0
DL1
SS
ST00
ST01
ST10
ST11
D00
D01
D02
D03
D04
D10
D11
D12
D13
D14
12V
0V
5V
8V
2V
PROGRAM SELECTED DATA LINE
PROGRAM UNSELECTED DATA LINE
PROGRAM SELECTED DATA LINE
PROGRAM UNSELECTED DATA LINE
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11

FIG. 49

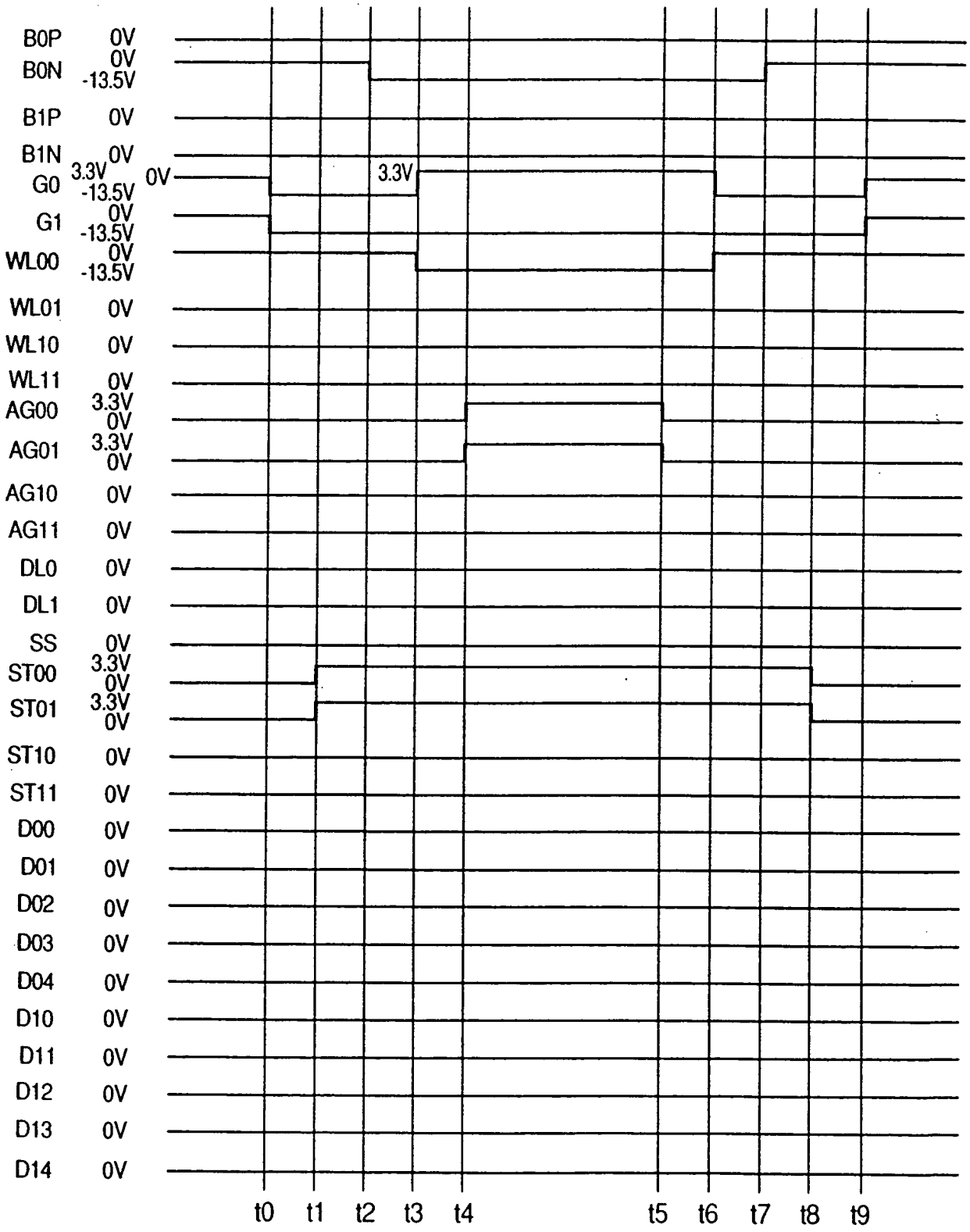

B0P 0V
B0N 0V -13.5V
B1P 0V
B1N 0V
G0 3.3V 0V -13.5V
G1 0V -13.5V
WL00 0V -13.5V
WL01 0V
WL10 0V
WL11 0V
AG00 3.3V 0V
AG01 3.3V 0V
AG10 0V
AG11 0V
DL0 0V
DL1 0V
SS 0V
ST00 3.3V 0V
ST01 3.3V 0V
ST10 0V
ST11 0V
D00 0V
D01 0V
D02 0V
D03 0V
D04 0V
D10 0V
D11 0V
D12 0V
D13 0V
D14 0V
3.3V
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9

FIG. 50

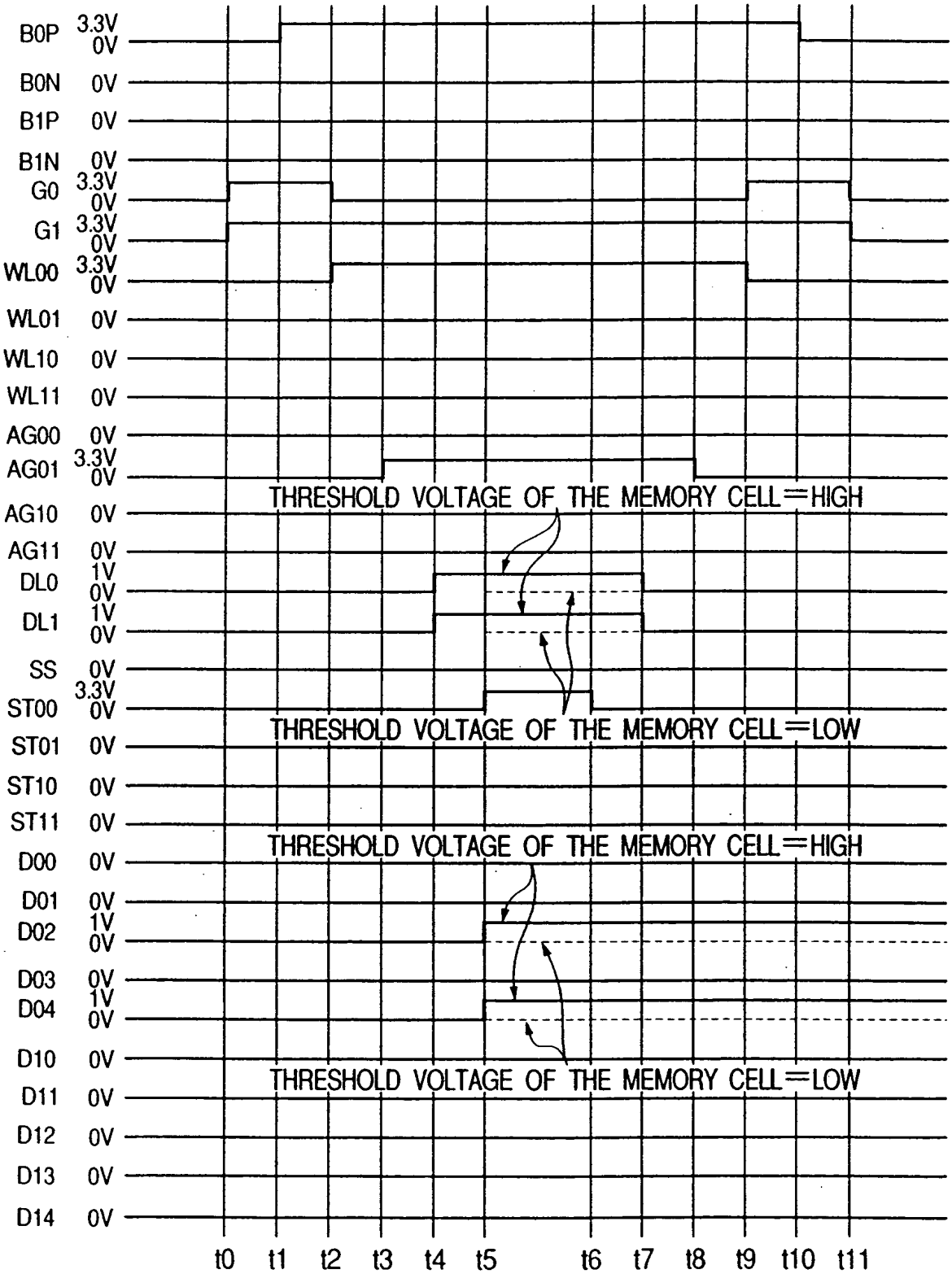

B0P 3.3V 0V
B0N 0V
B1P 0V
B1N 0V
G0 3.3V 0V
G1 3.3V 0V
WL00 3.3V 0V
WL01 0V
WL10 0V
WL11 0V
AG00 0V
AG01 3.3V 0V
AG10 0V
AG11 0V
DL0 1V 0V
DL1 1V 0V
SS 0V
ST00 3.3V 0V
ST01 0V
ST10 0V
ST11 0V
D00 0V
D01 0V
D02 1V 0V
D03 0V
D04 1V 0V
D10 0V
D11 0V
D12 0V
D13 0V
D14 0V
THRESHOLD VOLTAGE OF THE MEMORY CELL=HIGH
THRESHOLD VOLTAGE OF THE MEMORY CELL=LOW
THRESHOLD VOLTAGE OF THE MEMORY CELL=HIGH
THRESHOLD VOLTAGE OF THE MEMORY CELL=LOW
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11

FIG. 51

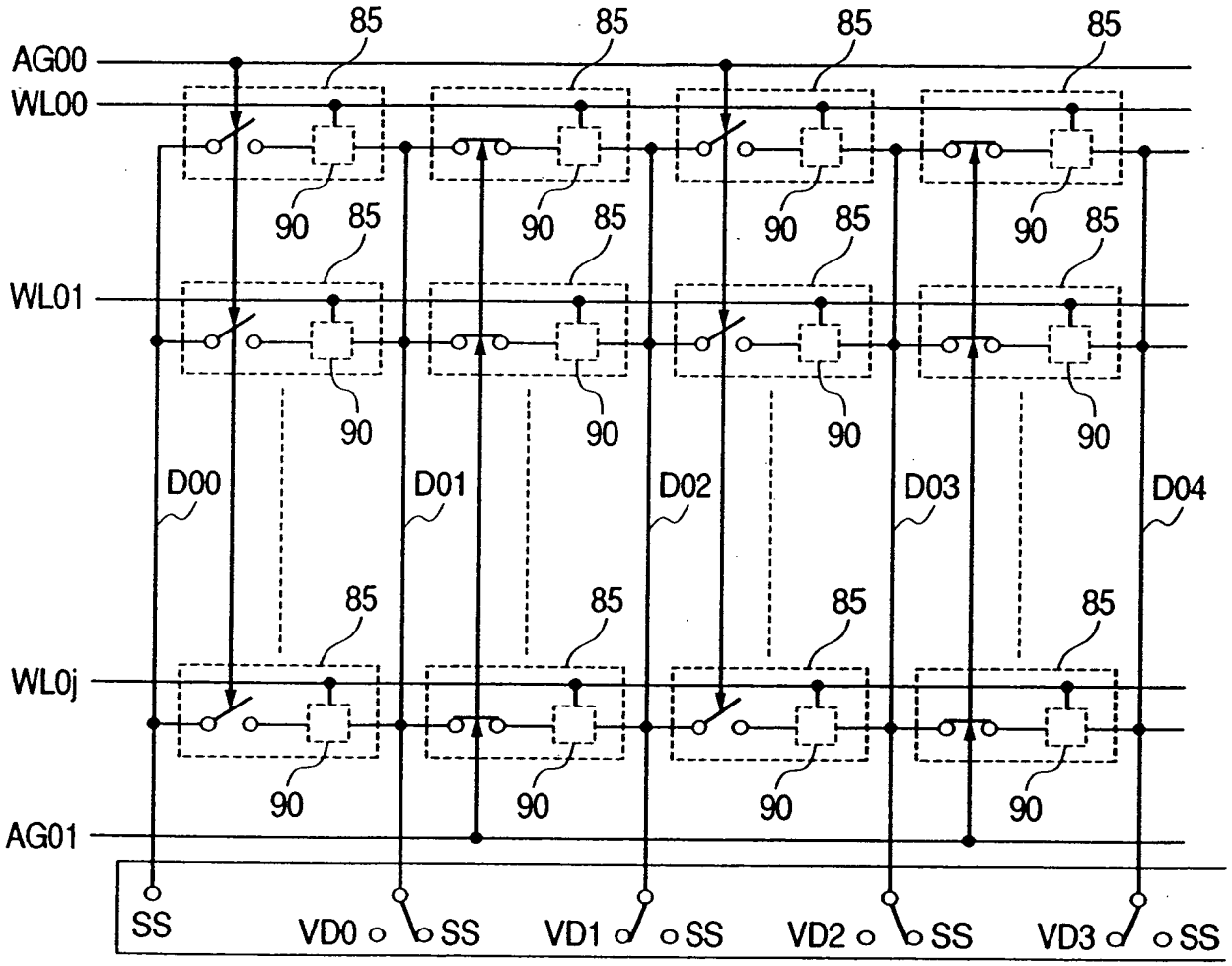

AG00
WL00
WL01
WL0j
AG01
85
90
D00
D01
D02
D03
D04
SS
VD0
VD1
VD2
VD3

FIG. 52A

WITH SELECT TRANSISTOR

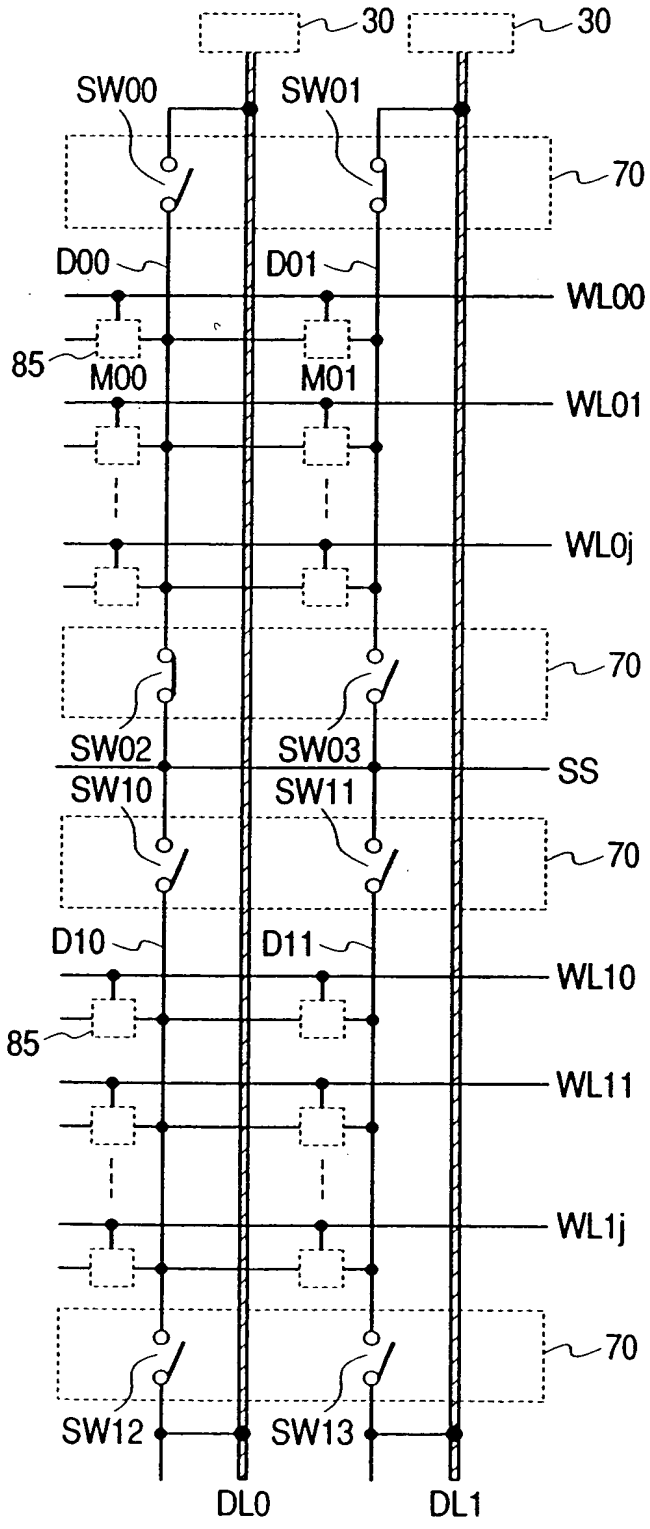


FIG. 52B

WITHOUT SELECT TRANSISTOR

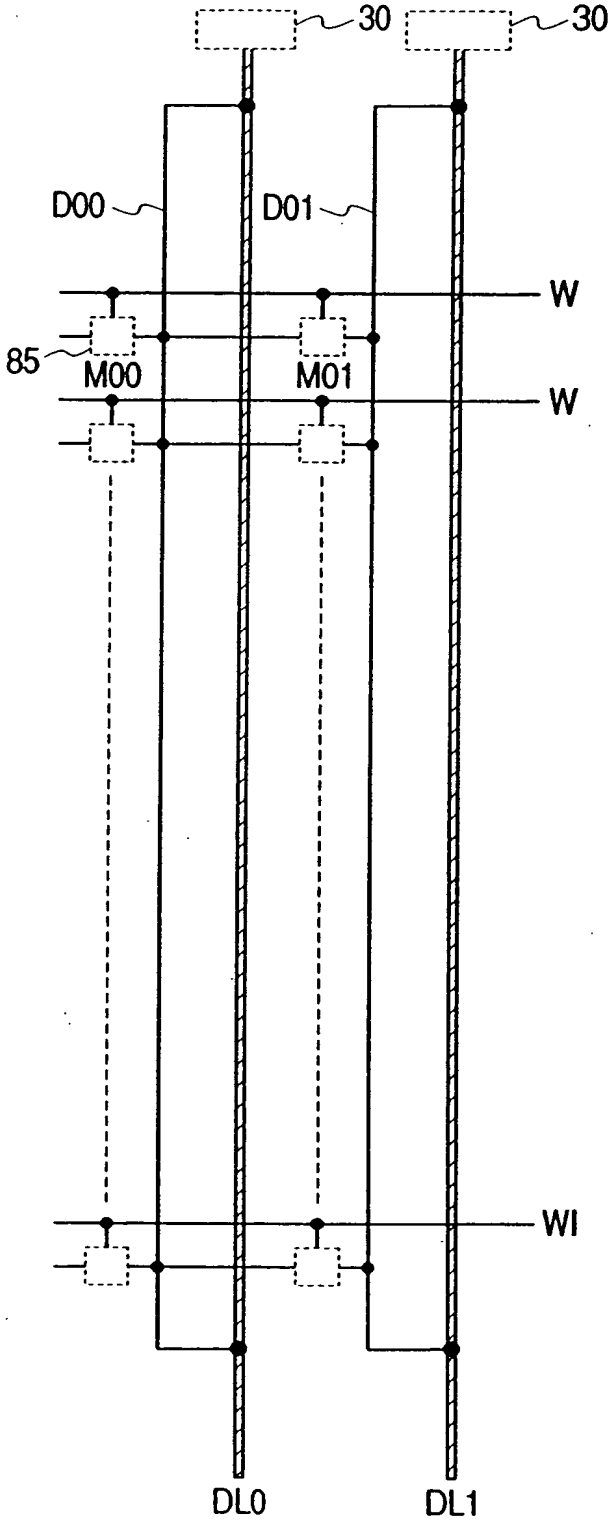


FIG. 53

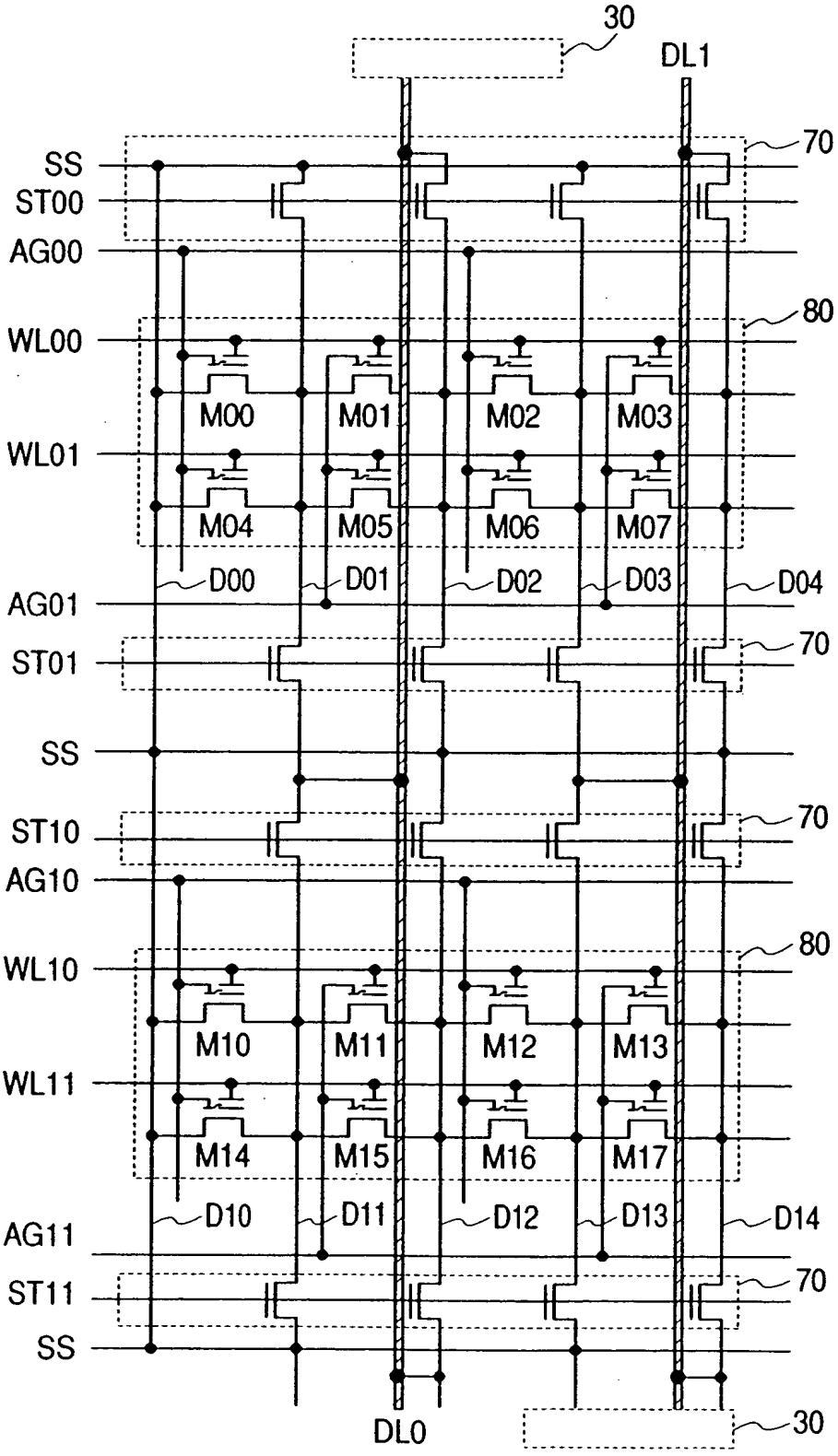

30
DL1
70
SS
ST00
AG00
80
WL00
M00
M01
M02
M03
WL01
M04
M05
M06
M07
D00
D01
D02
D03
D04
AG01
ST01
70
SS
ST10
70
AG10
80
WL10
M10
M11
M12
M13
WL11
M14
M15
M16
M17
D10
D11
D12
D13
D14
AG11
ST11
70
SS
DL0
30

FIG. 54

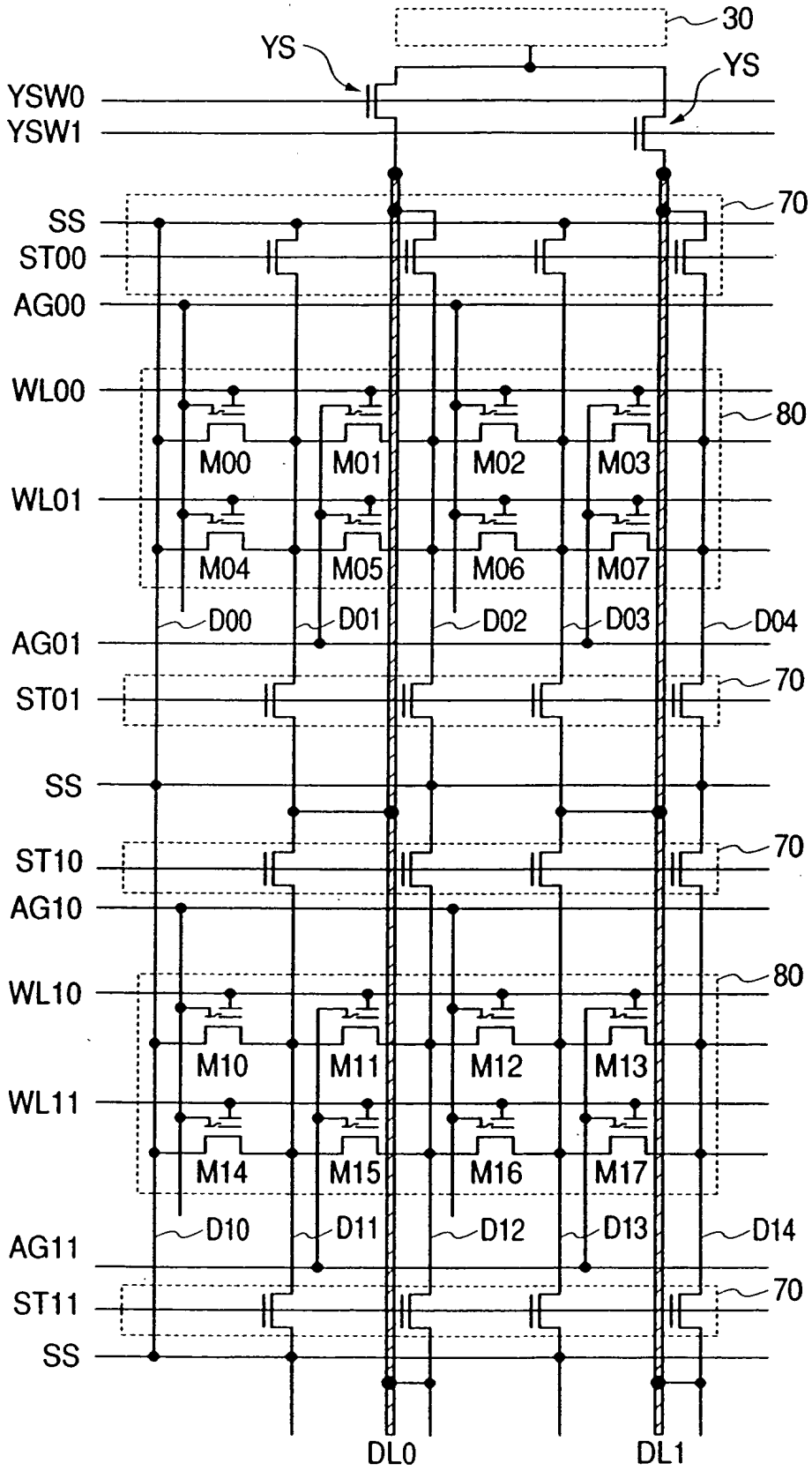

30
YS
YS
YSW0
YSW1
70
SS
ST00
AG00
WL00
80
M00
M01
M02
M03
WL01
M04
M05
M06
M07
D00
D01
D02
D03
D04
AG01
ST01
70
SS
ST10
70
AG10
WL10
80
M10
M11
M12
M13
WL11
M14
M15
M16
M17
D10
D11
D12
D13
D14
AG11
ST11
70
SS
DL0
DL1

FIG. 55

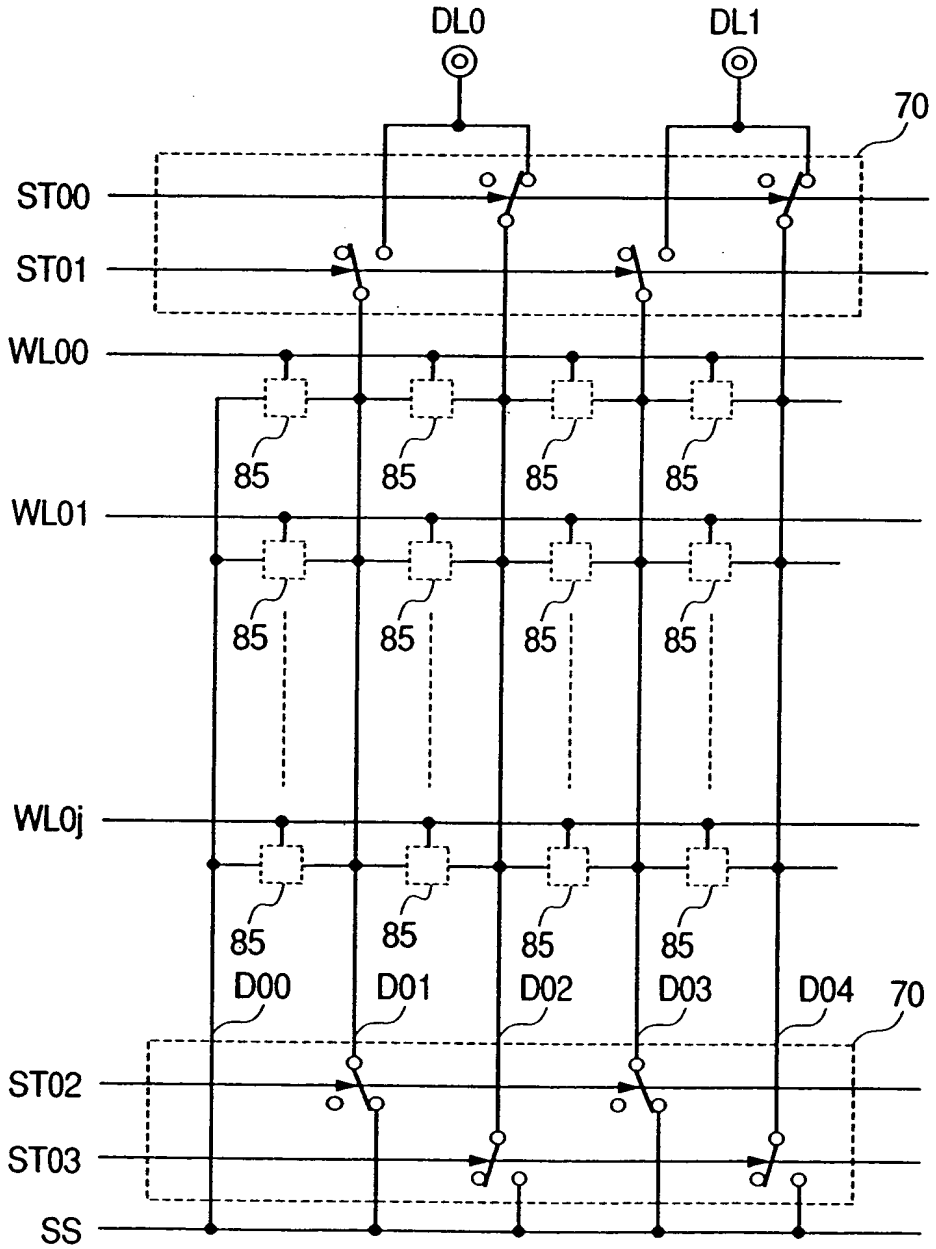

DL0
DL1
70
ST00
ST01
WL00
WL01
WL0j
85
D00
D01
D02
D03
D04
ST02
ST03
SS

FIG. 56

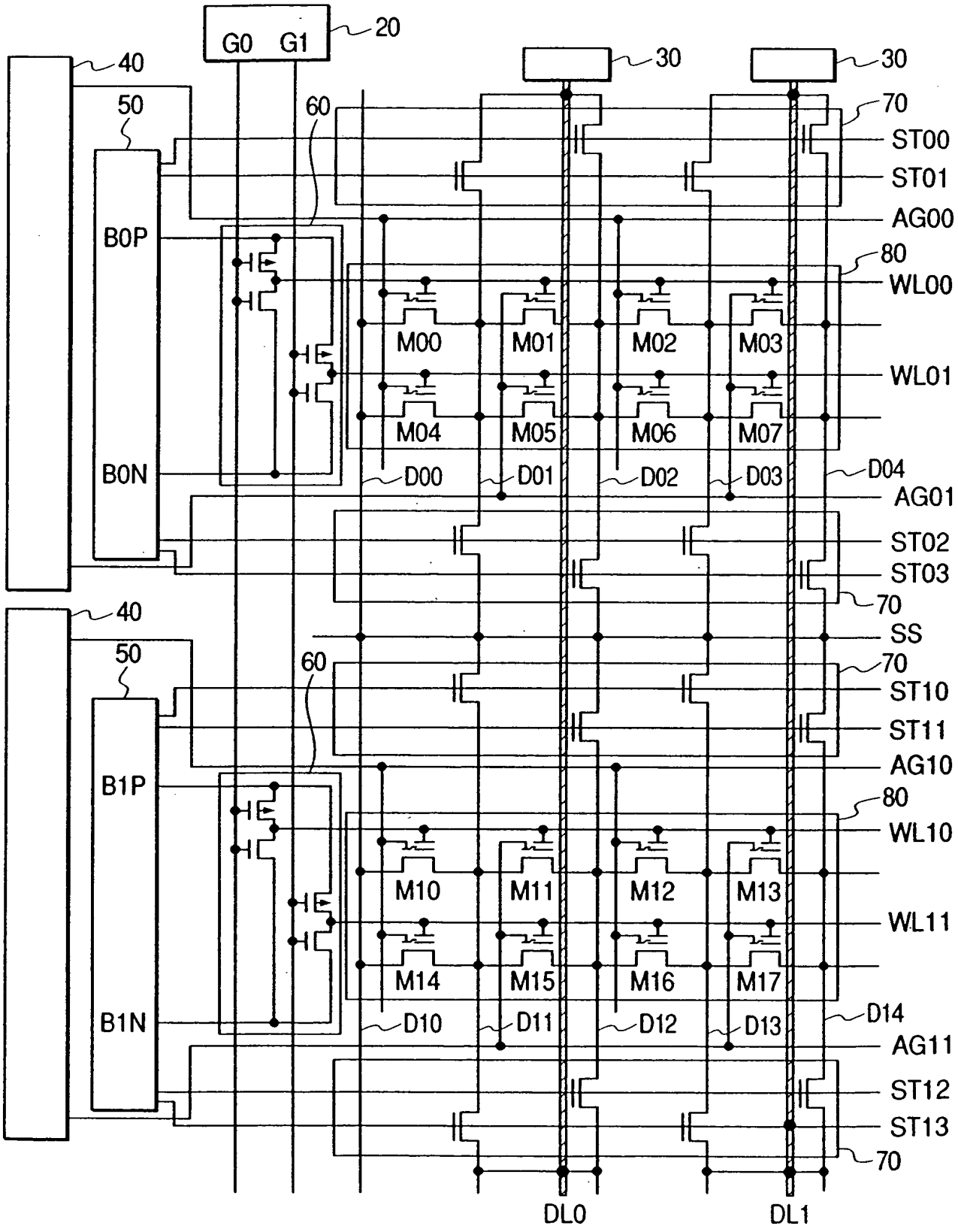

G0
G1
20
40
50
60
30
30
70
ST00
ST01
AG00
80
WL00
B0P
M00
M01
M02
M03
WL01
M04
M05
M06
M07
B0N
D00
D01
D02
D03
D04
AG01
ST02
ST03
70
40
SS
50
60
70
ST10
ST11
AG10
80
WL10
B1P
M10
M11
M12
M13
WL11
M14
M15
M16
M17
B1N
D10
D11
D12
D13
D14
AG11
ST12
ST13
70
DL0
DL1

FIG. 57

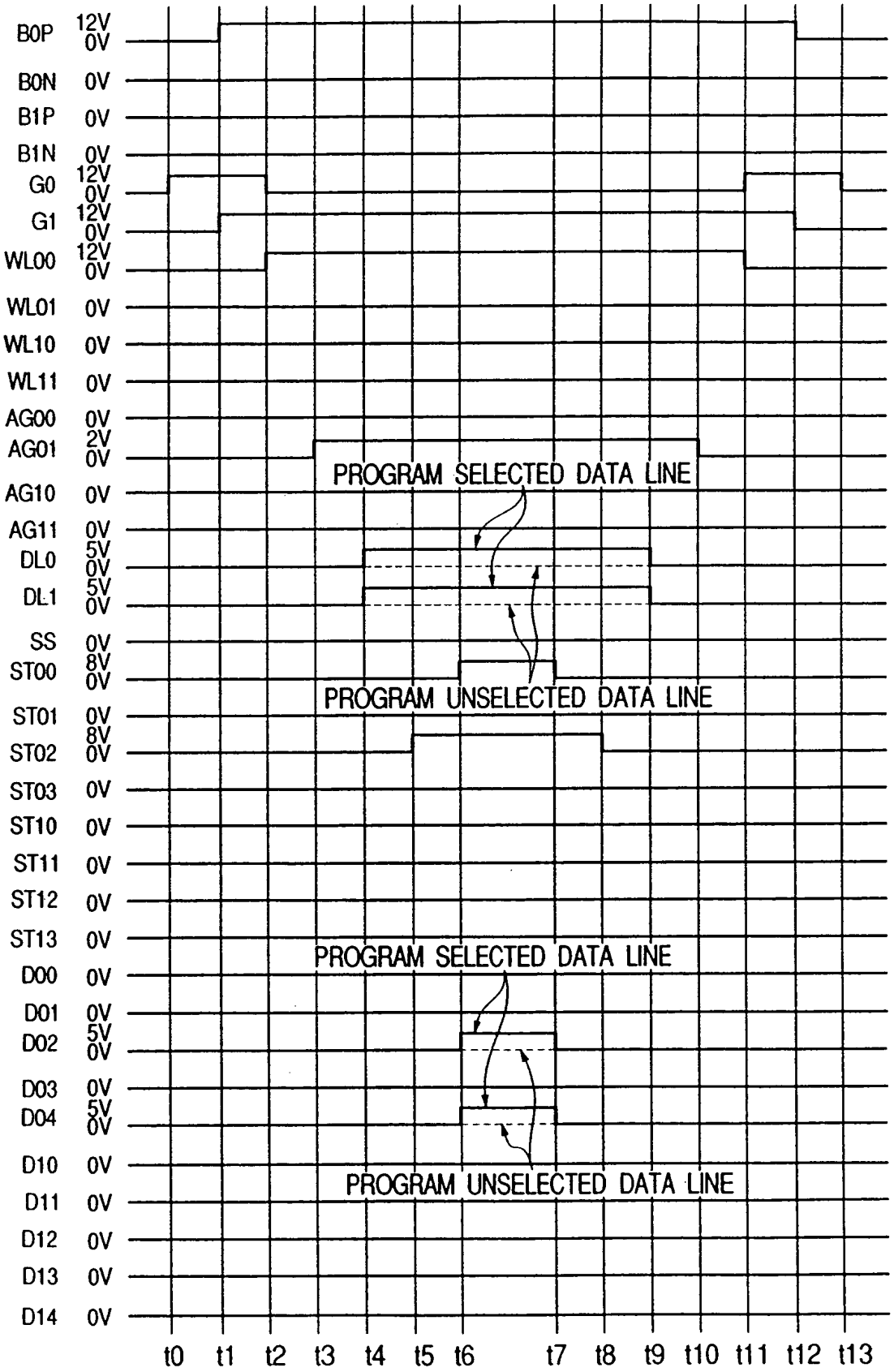

B0P 12V 0V
B0N 0V
B1P 0V
B1N 0V
G0 12V 0V
G1 12V 0V
WL00 12V 0V
WL01 0V
WL10 0V
WL11 0V
AG00 0V
AG01 2V 0V
AG10 0V
AG11 0V
DL0 5V 0V
DL1 5V 0V
SS 0V
ST00 8V 0V
ST01 0V
ST02 8V 0V
ST03 0V
ST10 0V
ST11 0V
ST12 0V
ST13 0V
D00 0V
D01 0V
D02 5V 0V
D03 0V
D04 5V 0V
D10 0V
D11 0V
D12 0V
D13 0V
D14 0V
PROGRAM SELECTED DATA LINE
PROGRAM UNSELECTED DATA LINE
PROGRAM SELECTED DATA LINE
PROGRAM UNSELECTED DATA LINE
t0 t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13

FIG. 58

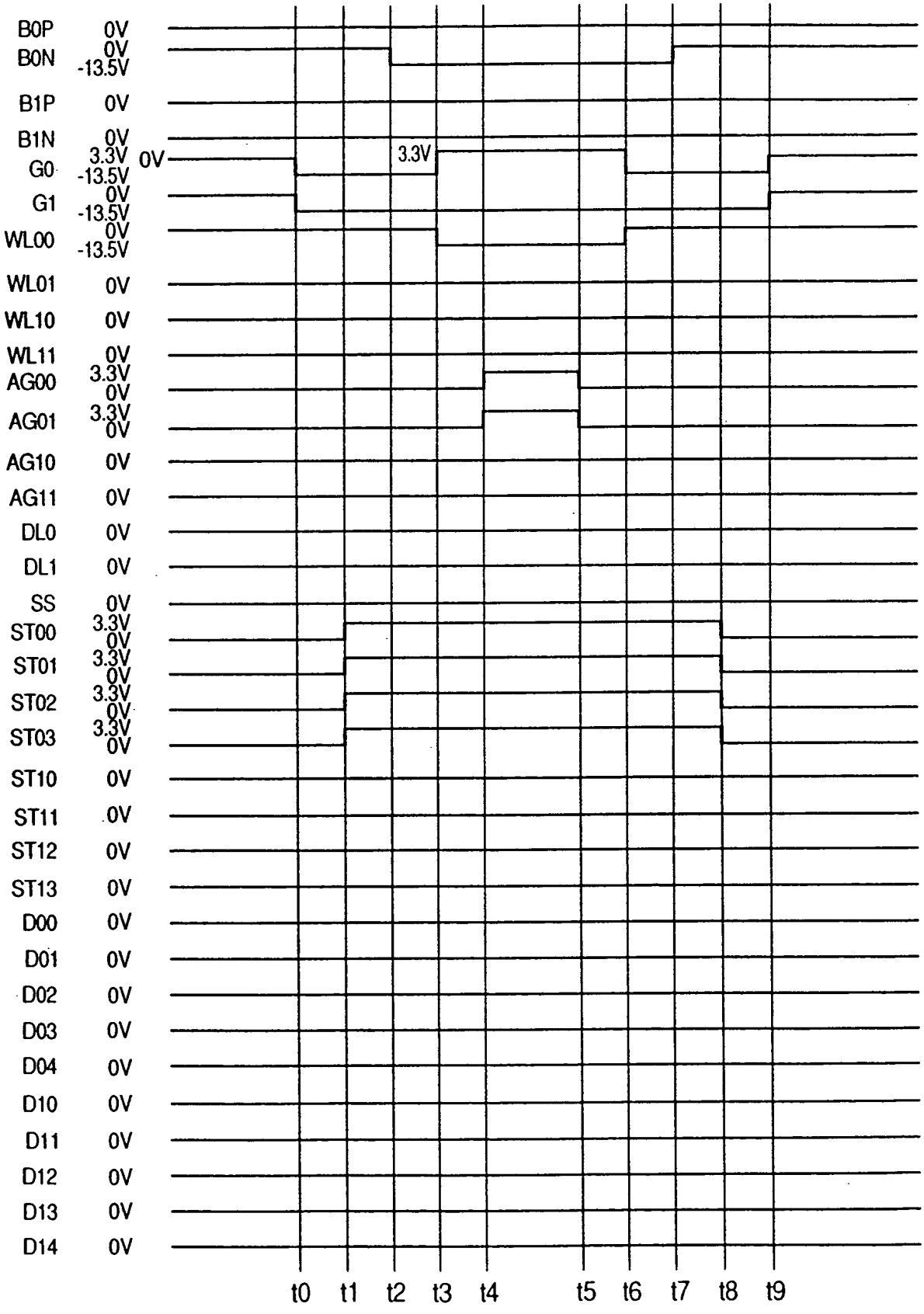

B0P
B0N
B1P
B1N
G0
G1
WL00
WL01
WL10
WL11
AG00
AG01
AG10
AG11
DL0
DL1
SS
ST00
ST01
ST02
ST03
ST10
ST11
ST12
ST13
D00
D01
D02
D03
D04
D10
D11
D12
D13
D14
0V
-13.5V
3.3V
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9

FIG. 59

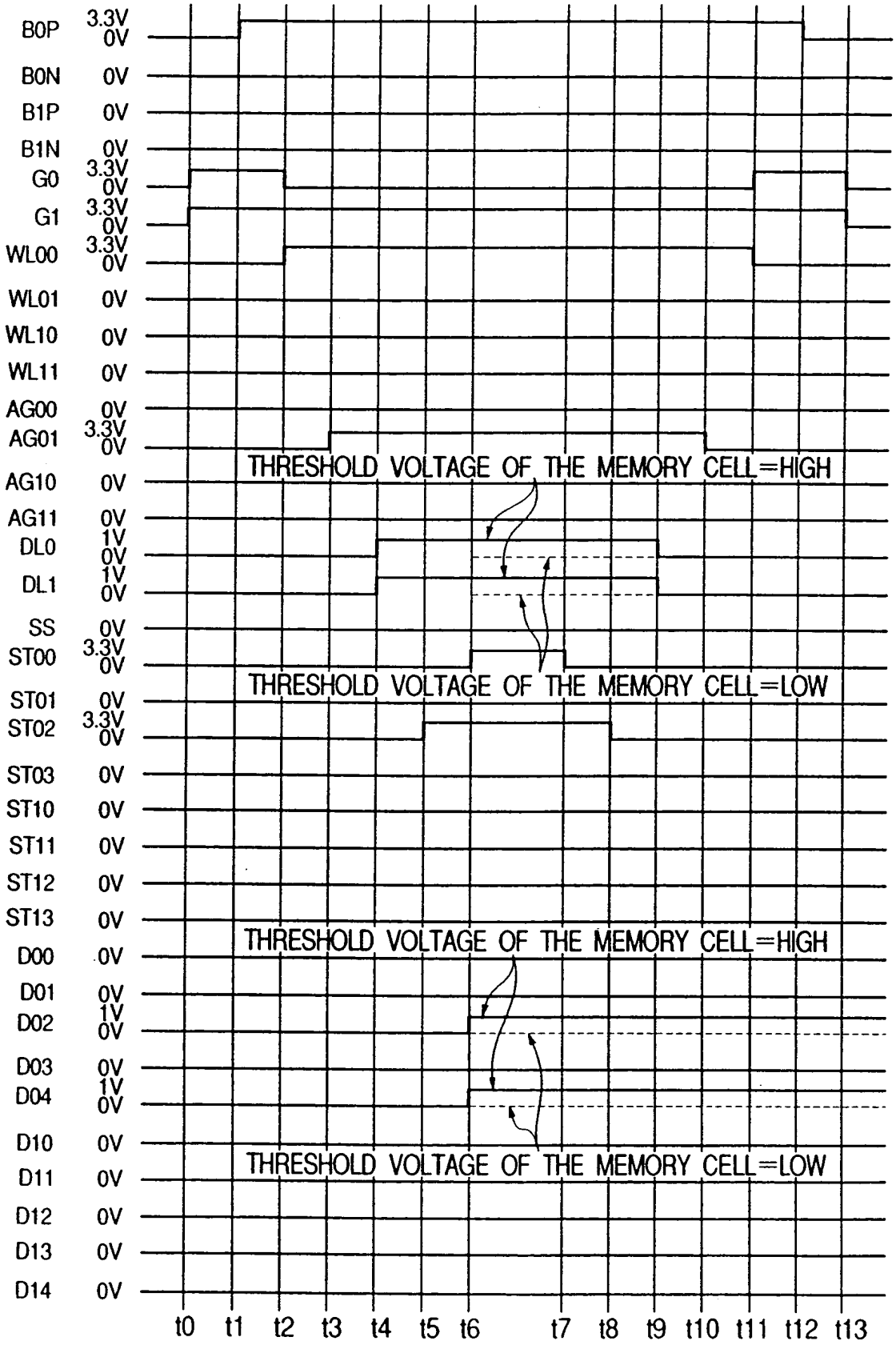

B0P
B0N
B1P
B1N
G0
G1
WL00
WL01
WL10
WL11
AG00
AG01
AG10
AG11
DL0
DL1
SS
ST00
ST01
ST02
ST03
ST10
ST11
ST12
ST13
D00
D01
D02
D03
D04
D10
D11
D12
D13
D14
3.3V
0V
1V
THRESHOLD VOLTAGE OF THE MEMORY CELL=HIGH
THRESHOLD VOLTAGE OF THE MEMORY CELL=LOW
THRESHOLD VOLTAGE OF THE MEMORY CELL=HIGH
THRESHOLD VOLTAGE OF THE MEMORY CELL=LOW
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13

FIG. 60

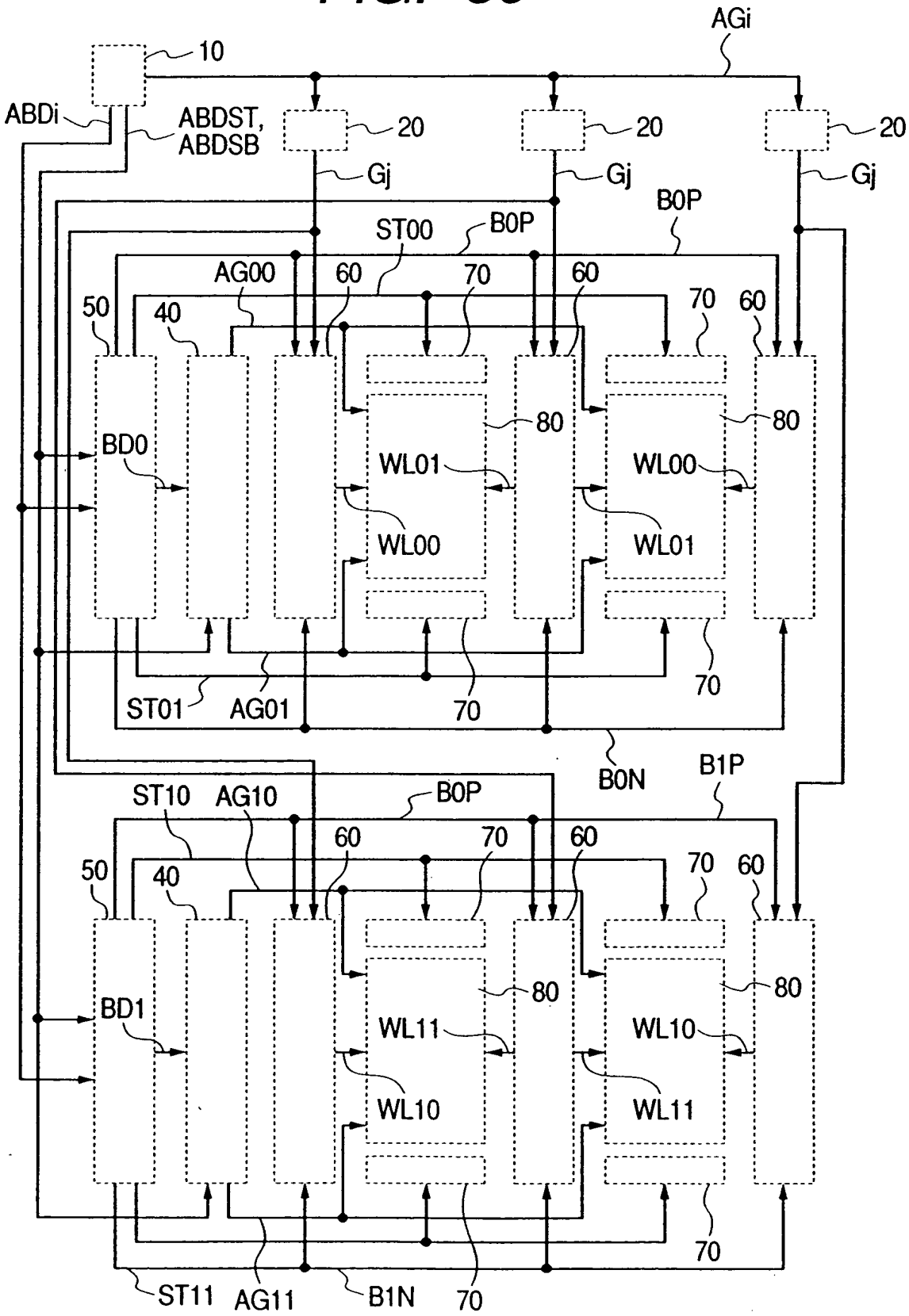

AGi
10
ABDi
ABDST,
ABDSB
20
20
20
Gj
Gj
Gj
B0P
ST00
B0P
AG00
60
70
60
70
60
50
40
80
80
BD0
WL01
WL00
WL00
WL01
70
ST01
AG01
70
B0N
B1P
ST10
AG10
B0P
60
70
60
70
60
50
40
80
80
BD1
WL11
WL10
WL10
WL11
70
ST11
AG11
B1N
70

FIG. 61

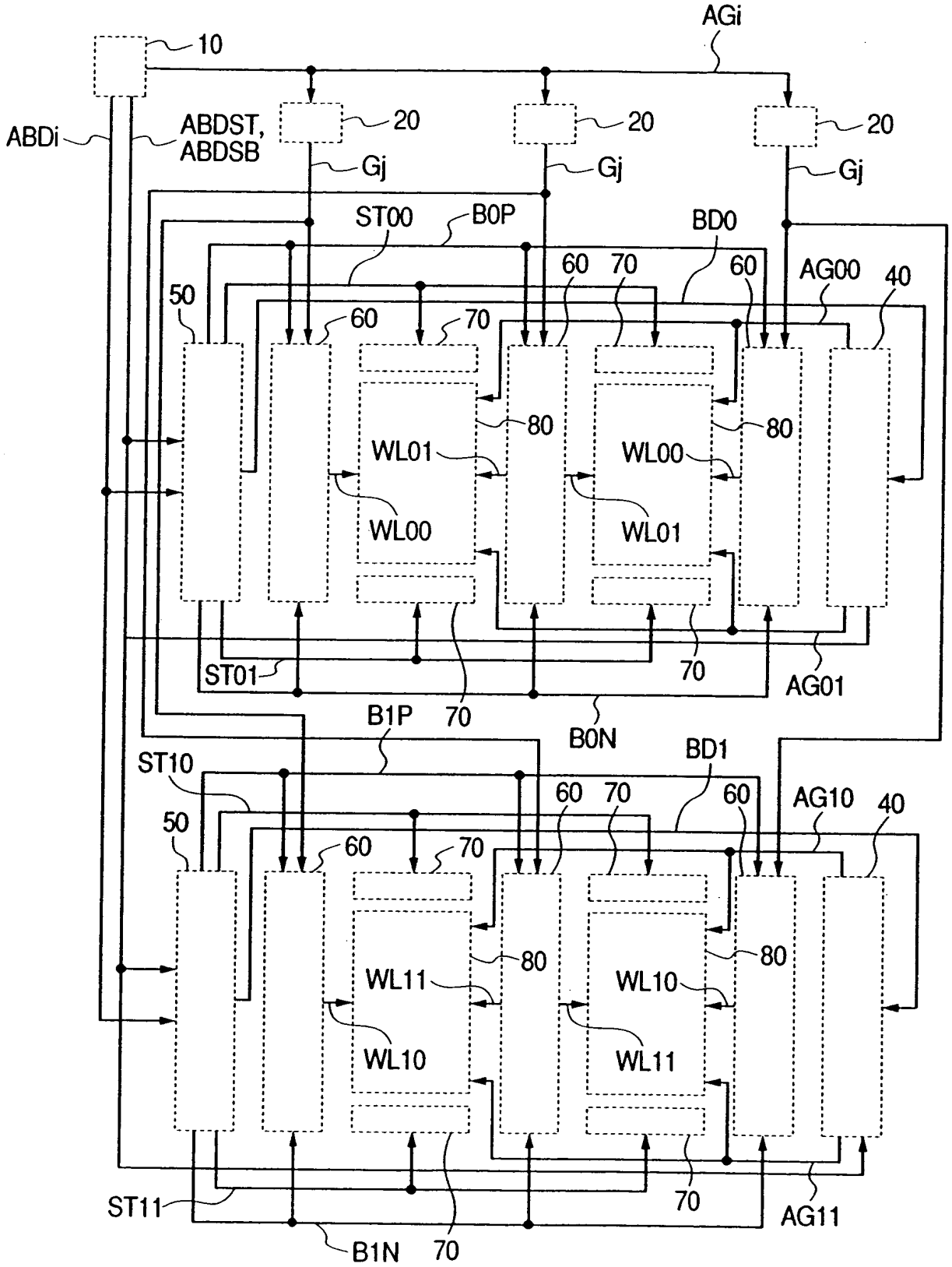

AGi
10
ABDi
ABDST,
ABDSB
20
20
20
Gj
Gj
Gj
ST00
B0P
BD0
60
70
60
AG00
40
50
60
70
80
80
WL01
WL00
WL00
WL01
70
ST01
AG01
B1P
70
B0N
BD1
ST10
60
70
60
AG10
40
50
60
70
80
80
WL11
WL10
WL10
WL11
70
ST11
AG11
B1N
70

FIG. 62

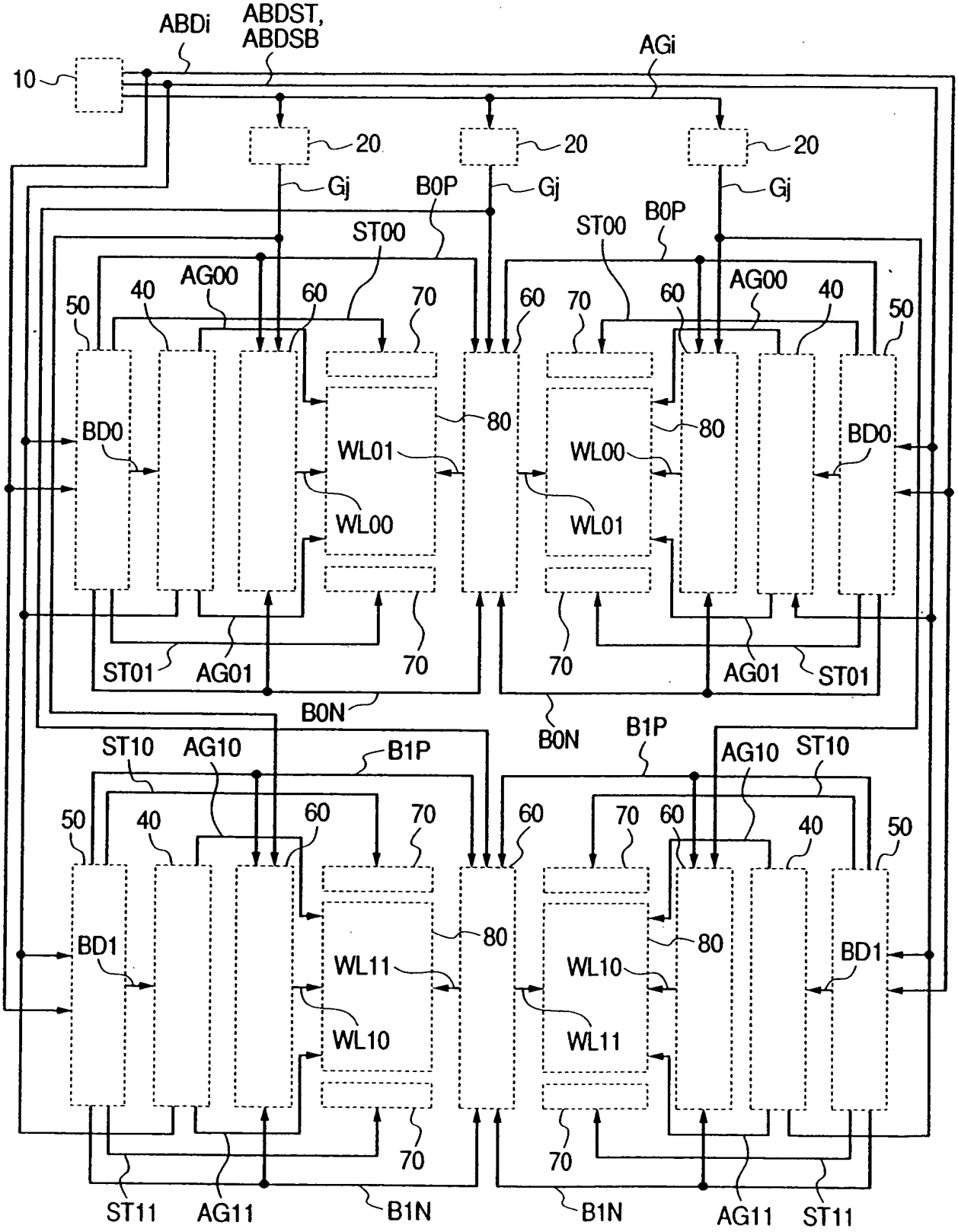

ABDi
ABDST,
ABDSB
AGi
10
20
20
20
Gj
B0P
Gj
Gj
ST00
ST00
B0P
AG00
AG00
40
40
50
50
60
60
70
60
70
60
70
80
80
BD0
BD0
WL01
WL00
WL00
WL01
ST01
AG01
70
70
AG01
ST01
B0N
B0N
B1P
B1P
ST10
AG10
AG10
ST10
50
50
40
40
60
60
70
70
60
70
80
80
BD1
BD1
WL11
WL10
WL10
WL11
70
70
ST11
AG11
B1N
B1N
AG11
ST11

FIG. 63

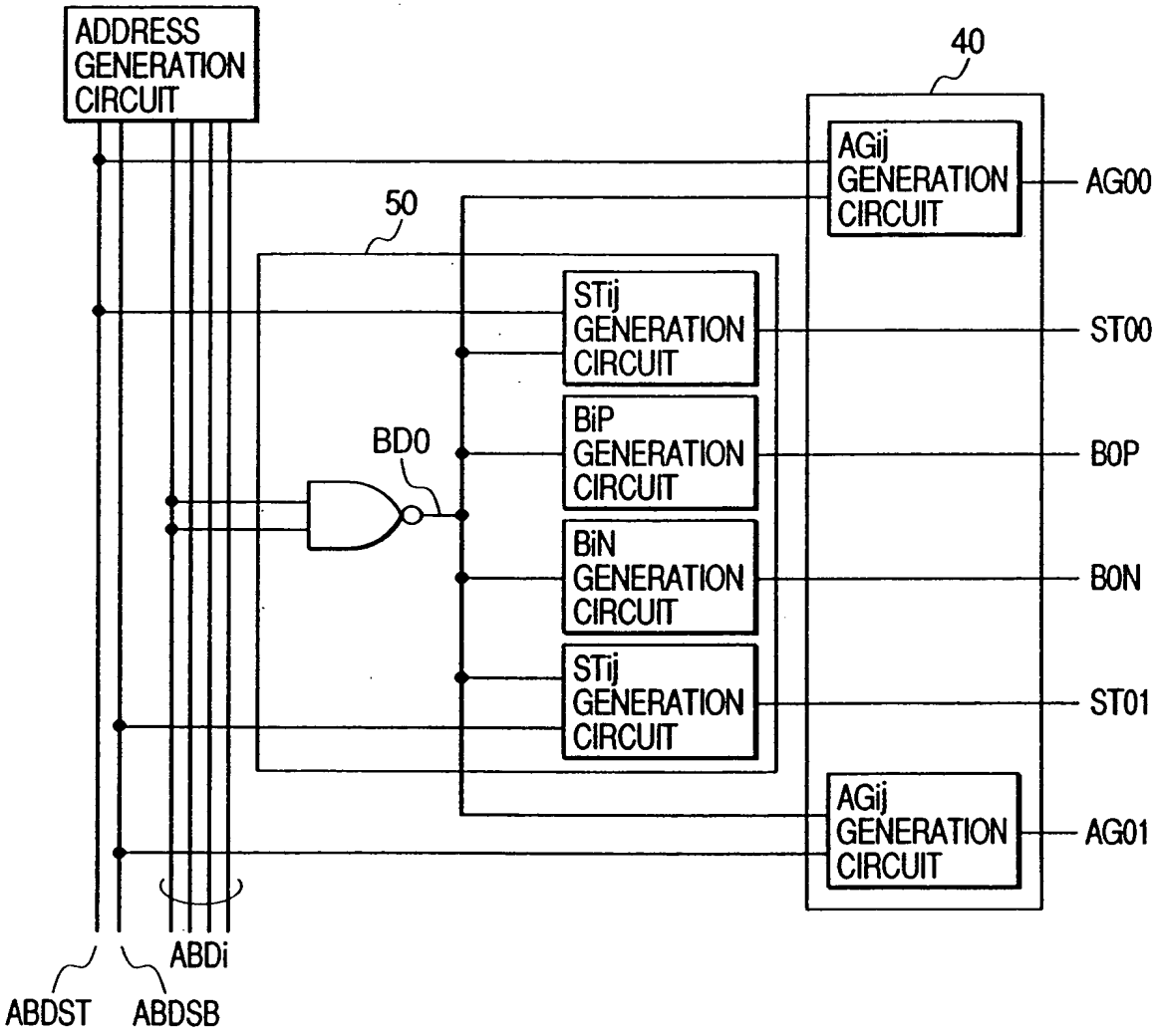

ADDRESS GENERATION CIRCUIT
40
AGij GENERATION CIRCUIT
AG00
50
STij GENERATION CIRCUIT
ST00
BiP GENERATION CIRCUIT
B0P
BD0
BiN GENERATION CIRCUIT
B0N
STij GENERATION CIRCUIT
ST01
AGij GENERATION CIRCUIT
AG01
ABDi
ABDST
ABDSB

FIG. 64

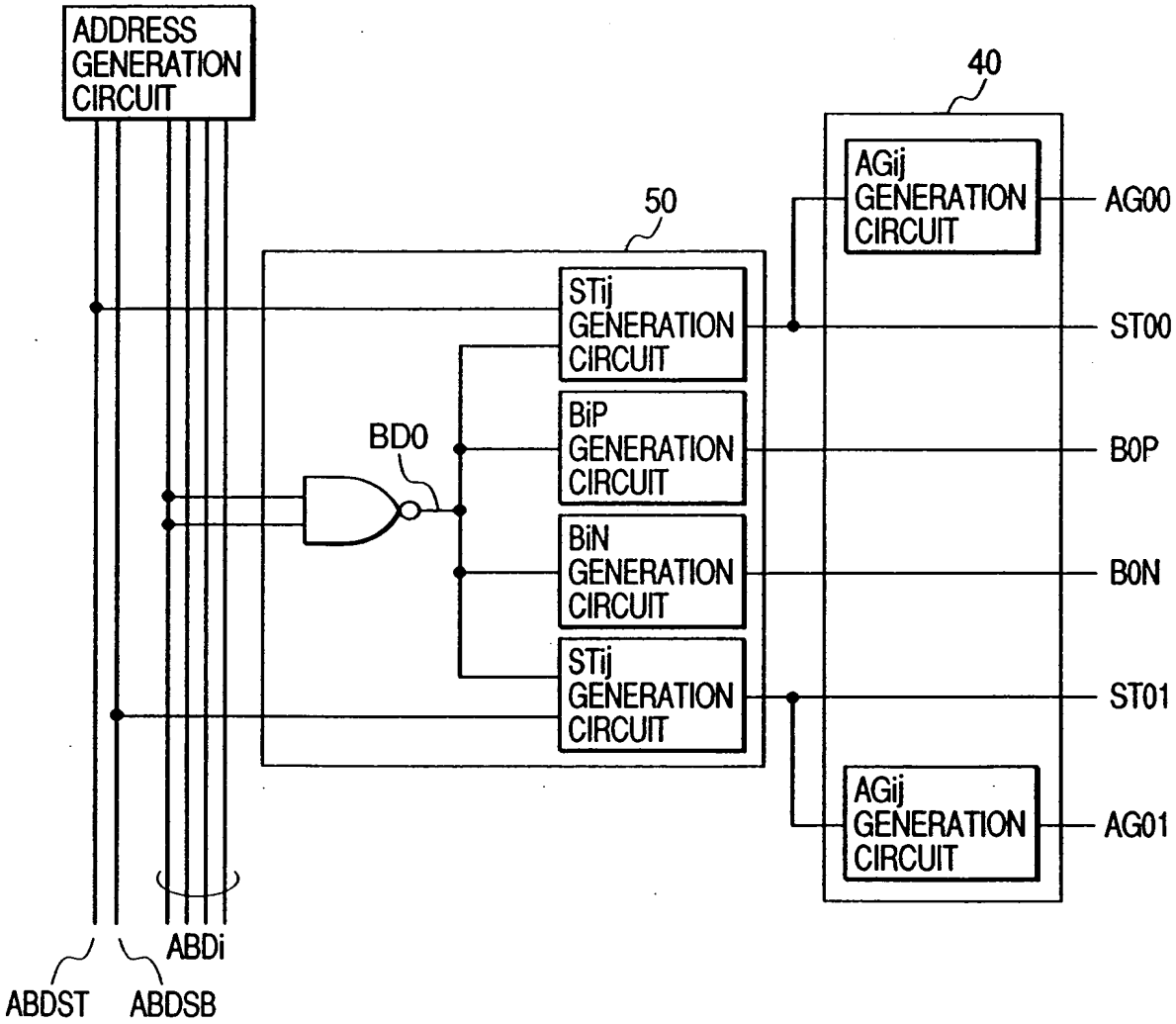

ADDRESS GENERATION CIRCUIT
40
AGij GENERATION CIRCUIT
AG00
50
STij GENERATION CIRCUIT
ST00
BiP GENERATION CIRCUIT
B0P
BD0
BiN GENERATION CIRCUIT
B0N
STij GENERATION CIRCUIT
ST01
AGij GENERATION CIRCUIT
AG01
ABDi
ABDST
ABDSB

FIG. 65

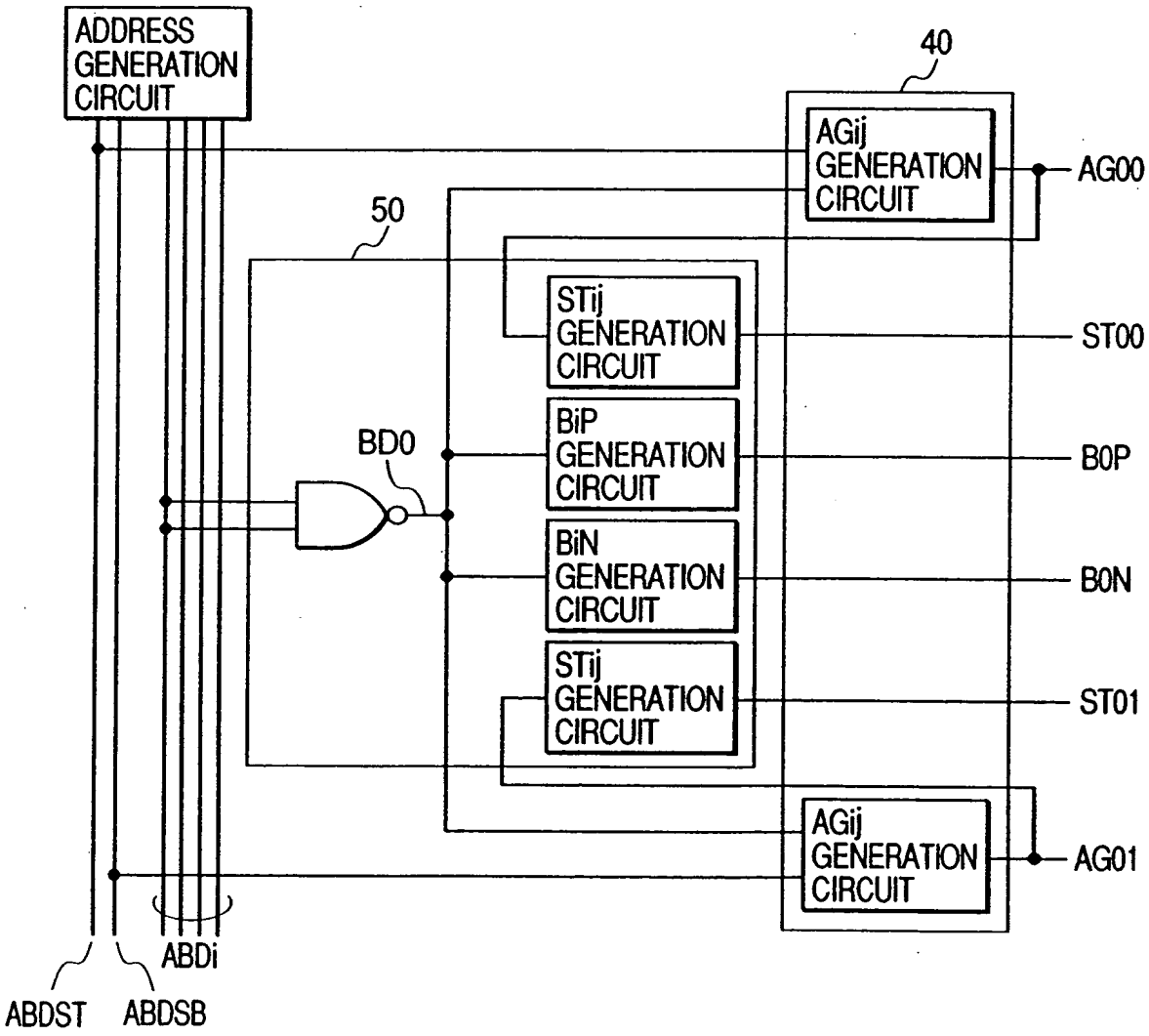

ADDRESS GENERATION CIRCUIT
40
AGij GENERATION CIRCUIT
AG00
50
STij GENERATION CIRCUIT
ST00
BiP GENERATION CIRCUIT
B0P
BD0
BiN GENERATION CIRCUIT
B0N
STij GENERATION CIRCUIT
ST01
AGij GENERATION CIRCUIT
AG01
ABDi
ABDST
ABDSB

FIG. 66

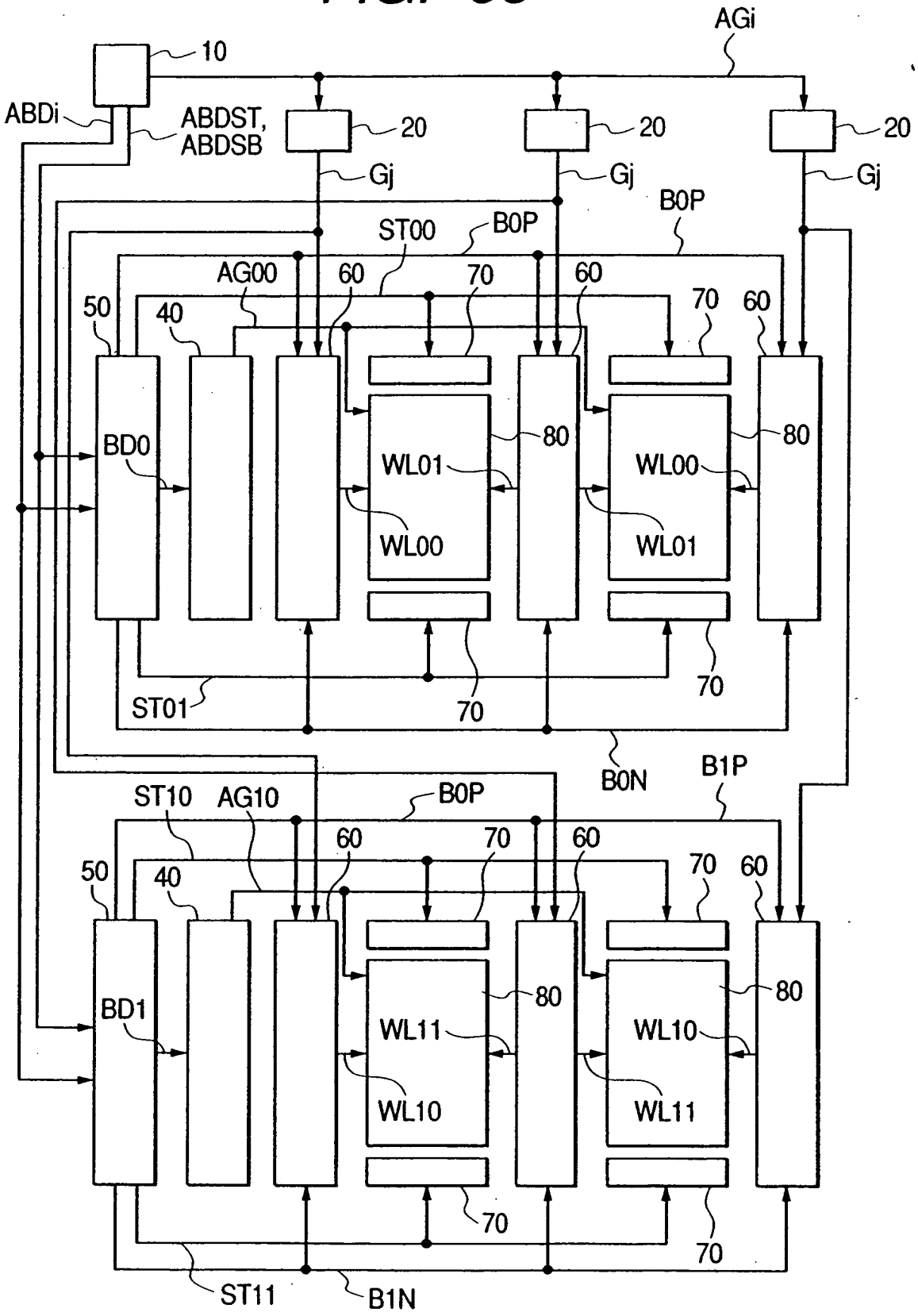

AGi
10
ABDi
ABDST,
ABDSB
20
20
20
Gj
Gj
Gj
B0P
ST00
B0P
AG00
60
70
60
70
60
50
40
BD0
WL01
80
WL00
80
WL00
WL01
70
70
ST01
70
B0N
B1P
ST10
AG10
B0P
60
70
60
70
60
50
40
BD1
WL11
80
WL10
80
WL10
WL11
70
70
ST11
B1N

FIG. 67

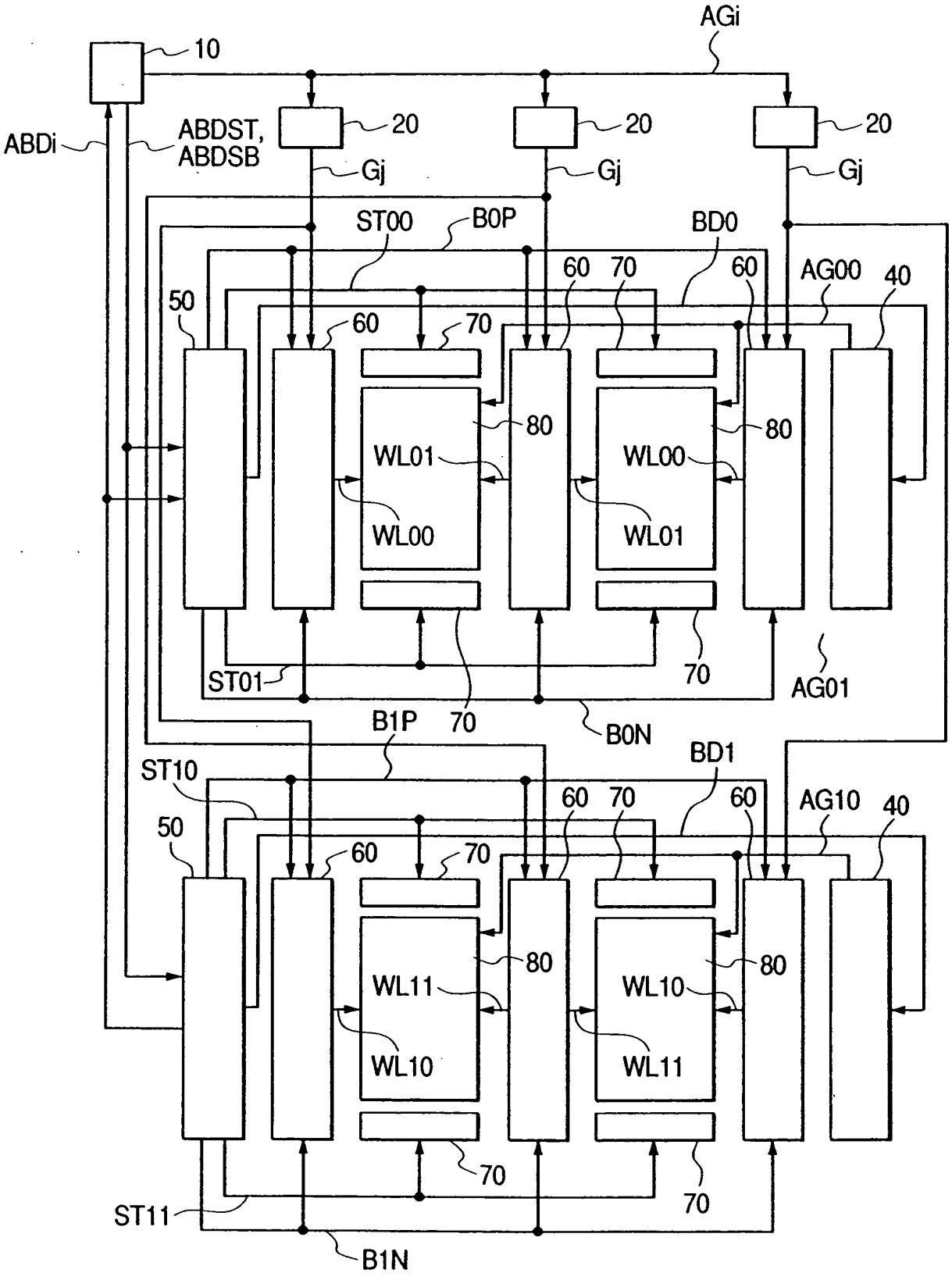

AGi
10
ABDi
ABDST,
ABDSB
20
20
20
Gj
Gj
Gj
ST00
B0P
BD0
60
70
60
AG00
40
50
60
70
80
80
WL01
WL00
WL00
WL01
70
AG01
ST01
70
B0N
B1P
BD1
ST10
60
70
60
AG10
40
50
60
70
80
80
WL11
WL10
WL10
WL11
70
70
ST11
B1N

FIG. 68

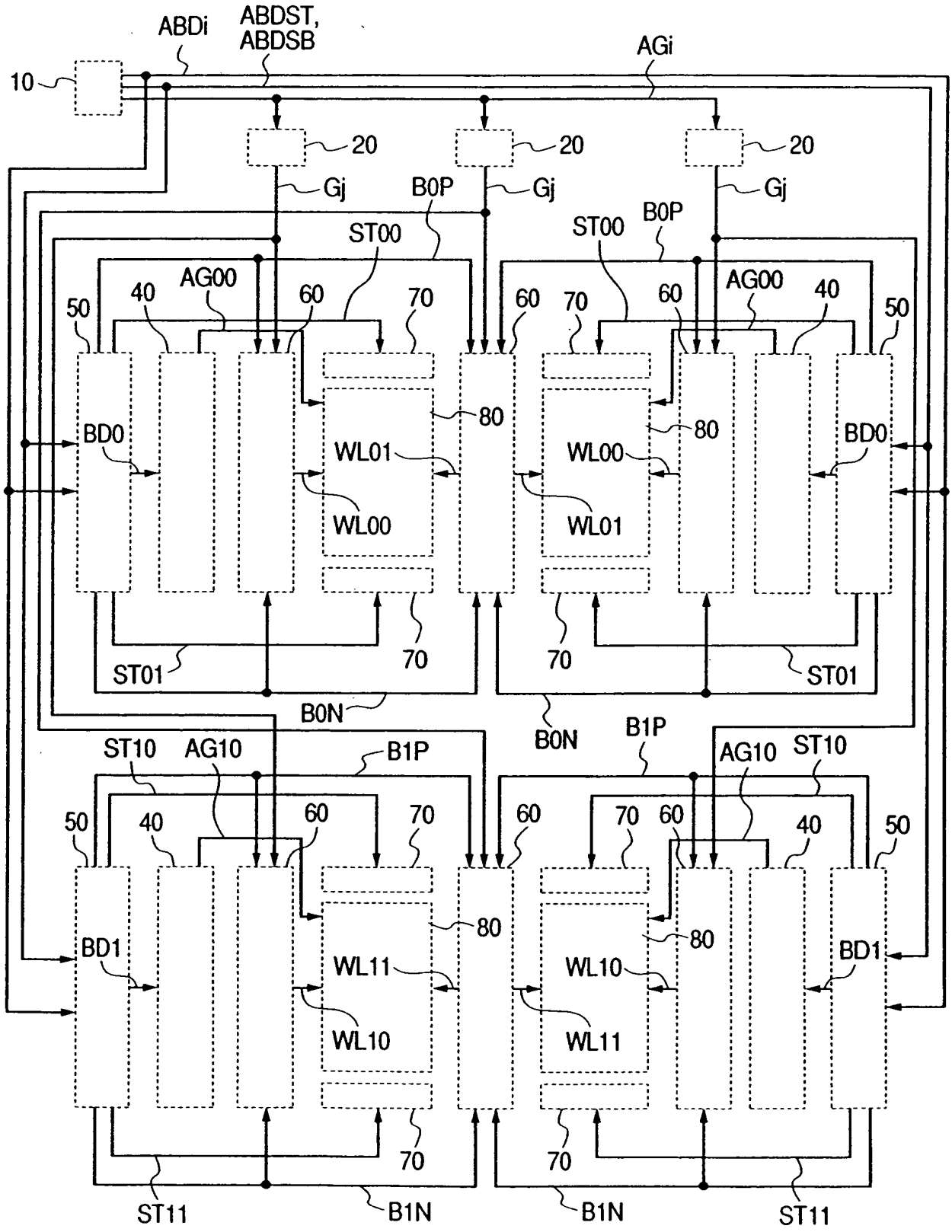

ABDi
ABDST,
ABDSB
AGi
10
20
20
20
Gj
B0P
Gj
Gj
ST00
B0P
ST00
B0P
AG00
40
60
70
60
70
60
AG00
40
50
50
BD0
80
WL01
WL00
80
WL00
WL01
BD0
70
70
70
ST01
ST01
B0N
B0N
B1P
ST10
AG10
B1P
AG10
ST10
50
40
60
70
60
70
60
40
50
BD1
80
WL11
WL10
80
WL10
WL11
BD1
70
70
ST11
B1N
B1N
ST11

FIG. 69

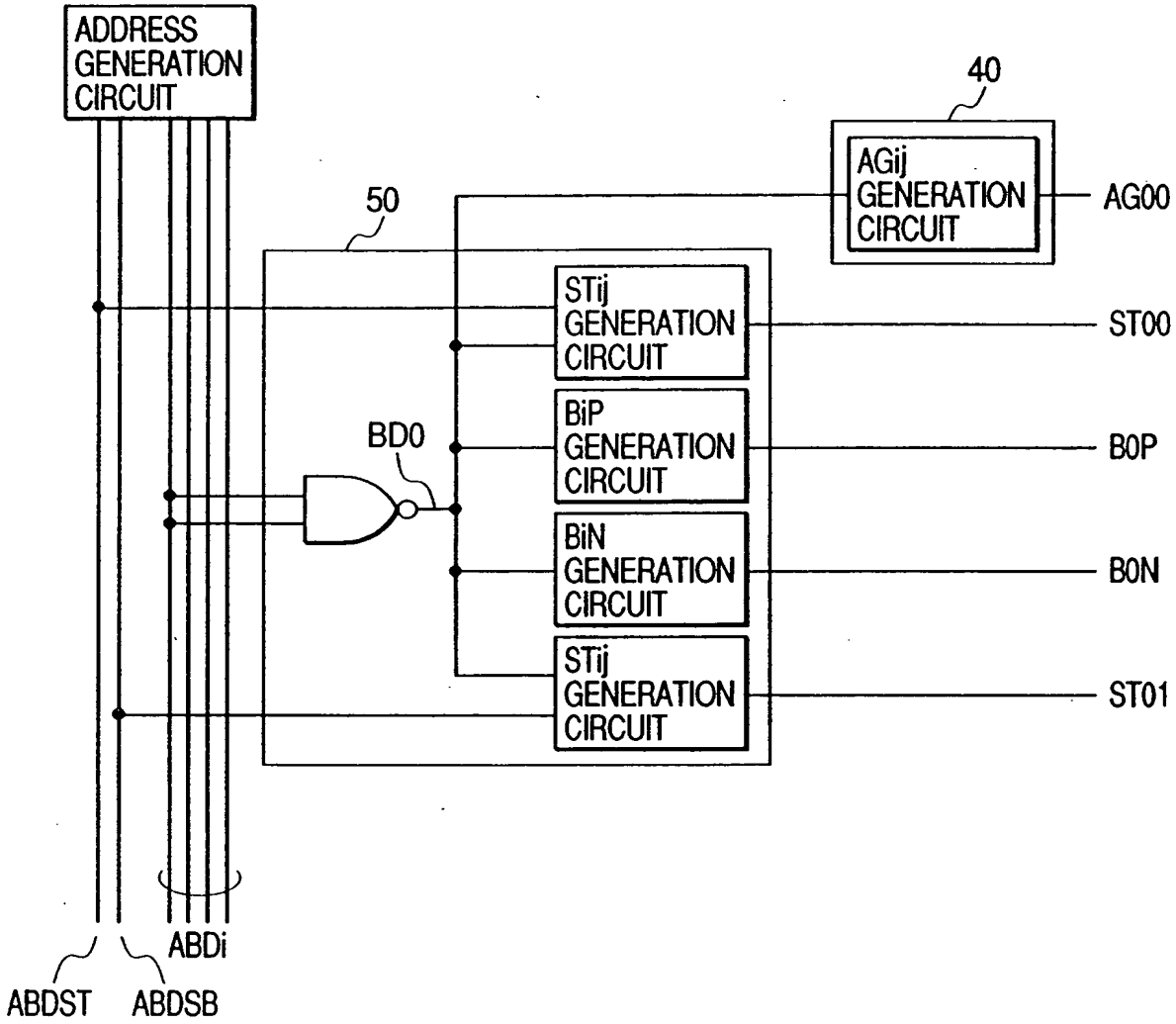
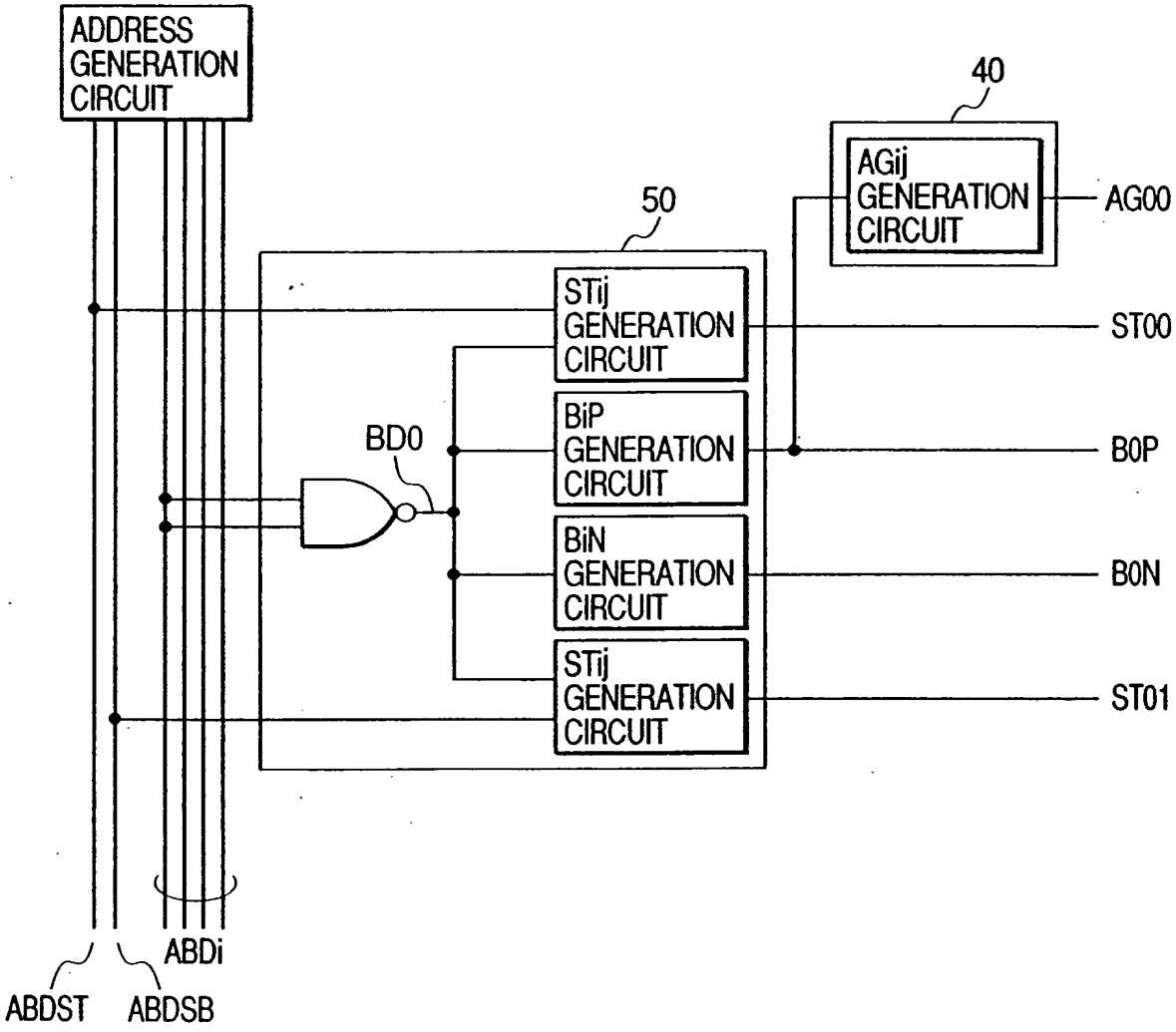

ADDRESS GENERATION CIRCUIT
40
AGij GENERATION CIRCUIT
AG00
50
STij GENERATION CIRCUIT
ST00
BiP GENERATION CIRCUIT
B0P
BD0
BiN GENERATION CIRCUIT
B0N
STij GENERATION CIRCUIT
ST01
ABDi
ABDST
ABDSB

FIG. 70


ADDRESS GENERATION CIRCUIT
40
AGij GENERATION CIRCUIT
AG00
50
STij GENERATION CIRCUIT
ST00
BiP GENERATION CIRCUIT
B0P
BD0
BiN GENERATION CIRCUIT
B0N
STij GENERATION CIRCUIT
ST01
ABDi
ABDST
ABDSB